

Product Overview

The NCA1043 high-speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller.

The NCA1043 offers excellent ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, very low power consumption, and passive behavior when the supply voltage is turned off. Advanced features include:

- Low-power management controls the power supply throughout the node while supporting local and remote wake-up with wake-up source recognition
- Several protection and diagnostic functions including bus line short-circuit detection and battery connection detection
- Can be interfaced directly to microcontrollers with supply voltages from 3 V to 5 V

The NCA1043 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the NCA1043 the ideal choice for high speed CAN networks containing nodes that need to be available all times, even when the internal VIO and VCC supplies are switched off.

Applications

- 12-V or 24-V System applications
- Automotive and transportation
 - Advanced driver assistance system (ADAS)
 - Infotainment
 - Cluster
 - Body electronics & lighting

Device Information

Part Number	Package	Body Size
NCA1043-Q1SPKR	SOP14	8.95mm × 3.90mm
NCA1043-Q1DNKR	DFN14	4.50mm × 3.00mm

Functional Block Diagrams

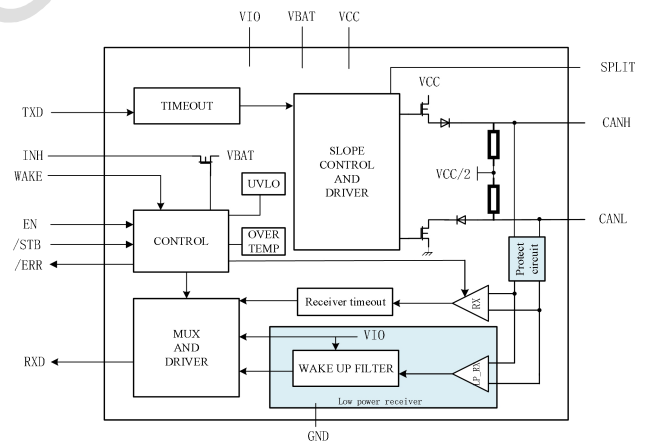


Figure 1. NCA1043 Block Diagram

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1. Pin Configuration and Functions

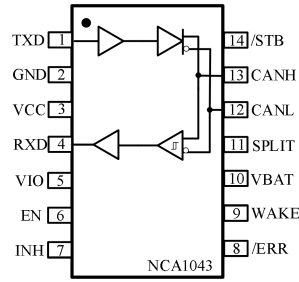


Figure 1.1 NCA1043 Package

Table 1.1 NCA1043 Pin Configuration and Description

NCA1043 PIN NO.	SYMBOL	FUNCTION
1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	Ground
3	VCC	Power Supply
4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	VIO	Logic I/O supply voltage
6	EN	enable control input
7	INH	inhibit output for switching external voltage regulators
8	/ERR	error and power-on indication output (active LOW)
9	WAKE	local wake-up input
10	VBAT	battery supply voltage
11	SPLIT	common-mode stabilization output
12	CANL	Low-level CAN bus line
13	CANH	High-level CAN bus line
14	/STB	STB (standby mode) select pin (active LOW)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Supply Voltage	VDD, VIO	-0.3		7	V	
	VBAT	-0.3		58	V	

I/O Voltage	TXD, RXD, STB_N,EN,E RR_N	-0.3		7	V	
	INH and WAKE	-0.3		58	V	
	Split, V_{CANH} , V_{CANL}	-58		58	V	
voltage between pin CANH and pin CANL	$V_{(CANH-CANL)}$	-20		20	V	
Current on pin WAKE	I_{WAKE}	-15			mA	
electrostatic discharge voltage	V_{ESD}	-8		8	kV	IEC 61000-4-2 (150 pF, 330 Ω) at pins CANH and CANL to GND
HBM	V_{ESD}	-8		8	kV	CANH and CANL
		-4		4	kV	Other pins
transient voltage	V_{trt}	-100			V	On pin CANH and CANL,SPLIT,VBAT, ISO 7637- 3 pulses 1
				75	V	On pin CANH and CANL, ,SPLIT,VBAT, ISO 7637- 3 pulses 2a
		-150			V	On pin CANH and CANL, ,SPLIT,VBAT, ISO 7637- 3 pulses 3a
				100	V	On pin CANH and CANL,,SPLIT,VBAT, ISO 7637- 3 pulses 3b
Operating Temperature	T_{opr}	-65		150	$^{\circ}\text{C}$	
Storage Temperature	T_{stg}	-40		150	$^{\circ}\text{C}$	

3. Recommended Operating Conditions

4. Thermal Information

5. Specifications

5.1. Electrical Characteristics

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Supply Voltage	V _{CC}	4.5		5.5	V	
	V _{uvd(vcc)}	3		4.3	V	undervoltage detection voltage on pin VCC
	V _{IO}	2.8		5.5	V	
	V _{uvd(vio)}	0.8		2.5	V	undervoltage detection voltage on pin VIO
supply current	I _{CC}			65	mA	TXD=0, R _L =60 Ω, normal mode
				109	mA	Normal mode, TXD=0, short circuit on bus lines: -3V < (V _{CANH} =V _{CANL}) < 18V
				9	mA	TXD=V _{IO} , normal mode or listen only mode
				4	uA	Standby or sleep mode
supply current on pin VIO	I _{IO}			500	uA	Normal mode, TXD=0, R _L =60 Ω
				4	uA	TXD=V _{IO} , normal or listen only mode
				5	uA	Standby or sleep mode
supply current on pin Vbat	I _{bat}			70	uA	Normal or listen only mode
			18	30	uA	Standby mode, V _{INH} =V _{WAKE} =V _{BAT} , V _{CC} >4.5V
			18	30	uA	sleep mode; V _{INH} =V _{CC} =V _{IO} =0, V _{WAKE} =V _{BAT}
Thermal-Shutdown Threshold	T _{TS}		190		°C	
Logic Side						
High level input voltage	V _{IH}	0.7*V _{IO}		V _{IO} +0.3	V	TXD & STB_N, EN pin
Low level input voltage	V _{IL}	-0.3		0.3*V _{IO}	V	TXD & STB_N, EN pin
High level input current	I _{IH}	-5		5	uA	TXD pin, V _{IN} =V _{IO}

High level input current	I_{IH}	1		10	uA	STB_N,EN pin, VIN=VIO
Low level input current	I_{IL}	-260		-30	uA	TXD pin, TXD=0
Low level input current	I_{IL}	-1		1	uA	STB_N,EN pin, VIN=0
Output High current	I_{OH}	-12	-3	-1	mA	RXD=VIO-0.4V
		-50	-3	-4	uA	ERR_N=VIO-0.4 VIO=VCC
Output Low current	I_{OL}	2	5	14	mA	RXD=0.4V
		0.1		2	mA	ERR_N=0.4V
Input Capacitance	C_{IN}		2		pF	TXD pin
PIN WAKE						
High level Input current	I_{IH}	-10		-1	uA	$V_{WAKE}=V_{BAT}-1.9V$
Low level Input current	I_{IL}	1		10	uA	$V_{WAKE}=V_{BAT}-3.1V$
Threshold voltage	V_{th}	$V_{BAT}-3$		$V_{BAT}-2$	V	$V_{STB_N}=0$
INH						
High level voltage drop	ΔV_H	0		0.8	V	IINH=-0.18mA
Leakage current	I_L	-2		2	uA	Sleep mode
SPLIT						
Output voltage	V_o	0.3V _{CC}		0.7V _{CC}	V	Normal or Listen-only mode; -500uA < I _{SPLIT} < 500uA
		0.45V _{CC}		0.55V _{CC}	V	Normal or Listen-only mode; RL=1M Ω
leakage current	I_L	-3		3	uA	Standby or Sleep mode; -58 V < V _{SPLIT} < +58 V
Driver						
CANH output voltage (Dominant)	$V_{OH(D)}$	2.75		4.5	V	VI=0V, R _{Load} =50 to 65Ω
CANL output voltage (Dominant)	$V_{OL(D)}$	0.5		2.25	V	VI=0V, R _{Load} =50 to 65Ω
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	-400		400	mV	$V_{dom(TX)sym}=V_{CC}-V_{CANH}-V_{CANL}$
transmitter voltage	V_{TXsym}	0.9V _{CC}		1.1V _{CC}	V	$V_{TXsym}=V_{CANH}+V_{CANL}$; f _{TXD} = 250 kHz, 1

symmetry						MHz and 2.5 MHz;
CAN bus output voltage (Recessive)	$V_{O(R)}$	2	2.5	3	V	$V_{TXD}=V_{IO}$, no load
		-0.1		0.1	V	Standby mode, no load
Differential output voltage(Dominant)	$V_{OD(D)}$	1.5		3	V	$V_{TXD}=0V$, $R_{Load}=45$ to 65Ω
		1.5		3.3	V	$V_{TXD}=0V$, $R_{Load}=45$ to 70Ω
		1.5		5		$V_{TXD}=0V$, $R_{Load}=2240\Omega$
Differential output voltage(Recessive)	$V_{OD(R)}$	-50		50	mV	Normal or listen only mode, $V_{TXD}=V_{IO}$
		-0.2		0.2	V	Standby or sleep mode
Common-mode output voltage	V_{OC}	2	2.5	3	V	
Peak-to-peak Common-mode output voltage	$V_{OC(PP)}$		250		mV	
Short-circuit output current	I_{OS}	-100		-40	mA	Test CANH, $TXD=0$, $V_{CANH}=-15V$ to $+40V$
		40		100	mA	Test CANL, $TXD=0$, $V_{CANL}=-15V$ to $+40V$
		-5	-0.4	5	mA	Normal mode; $V_{TXD}=V_{IO}$; $V_{CANH} = V_{CANL} = -27V$ to $+32V$
Receiver						
receiver recessive voltage	$V_{rec(RX)}$	-4		0.5	V	$-30V < V_{CANL} < +30V$; $-30V < V_{CANH} < +30V$; normal or listen only mode
		-4		0.4	V	$-30V < V_{CANL} < +30V$; $-30V < V_{CANH} < +30V$; standby or sleep mode
receiver dominant voltage	$V_{dom(RX)}$	0.9		9	V	$-30V < V_{CANL} < +30V$; $-30V < V_{CANH} < +30V$; normal or listen only mode
		1.15		9	V	$-30V < V_{CANL} < +30V$; $-30V < V_{CANH} < +30V$; standby or sleep mode
Hysteresis voltage	V_{HYS}	50	100	400	mV	$-30V < V_{CANL} < +30V$; $-30V < V_{CANH} < +30V$;
differential receiver threshold voltage	$V_{th(RX)dif}$	0.4		1.15	V	$-30V < V_{CANL} < +30V$; $-30V < V_{CANH} < +30V$;
Power-off (unpowered) bus input leakage current	$I_{OFF(LKG)}$	100		250	μA	$V_{CANH} = V_{CANL} = 5V$, $V_{CC} = 0V$
		-2		2	μA	$V_{CANH} = V_{CANL} = 5V$, $V_{BAT} = 0V$
		-2		2	μA	$V_{CC}=V_{IO}=V_{BAT} = 0V$ or $V_{CC}=V_{IO}=V_{BAT}$ =shorted to ground via $47k\Omega$; $V_{CANH} = V_{CANL} = 5V$
common-mode input capacitance	C_i		13	20	pF	
Differential input	C_{ID}		5	10	pF	

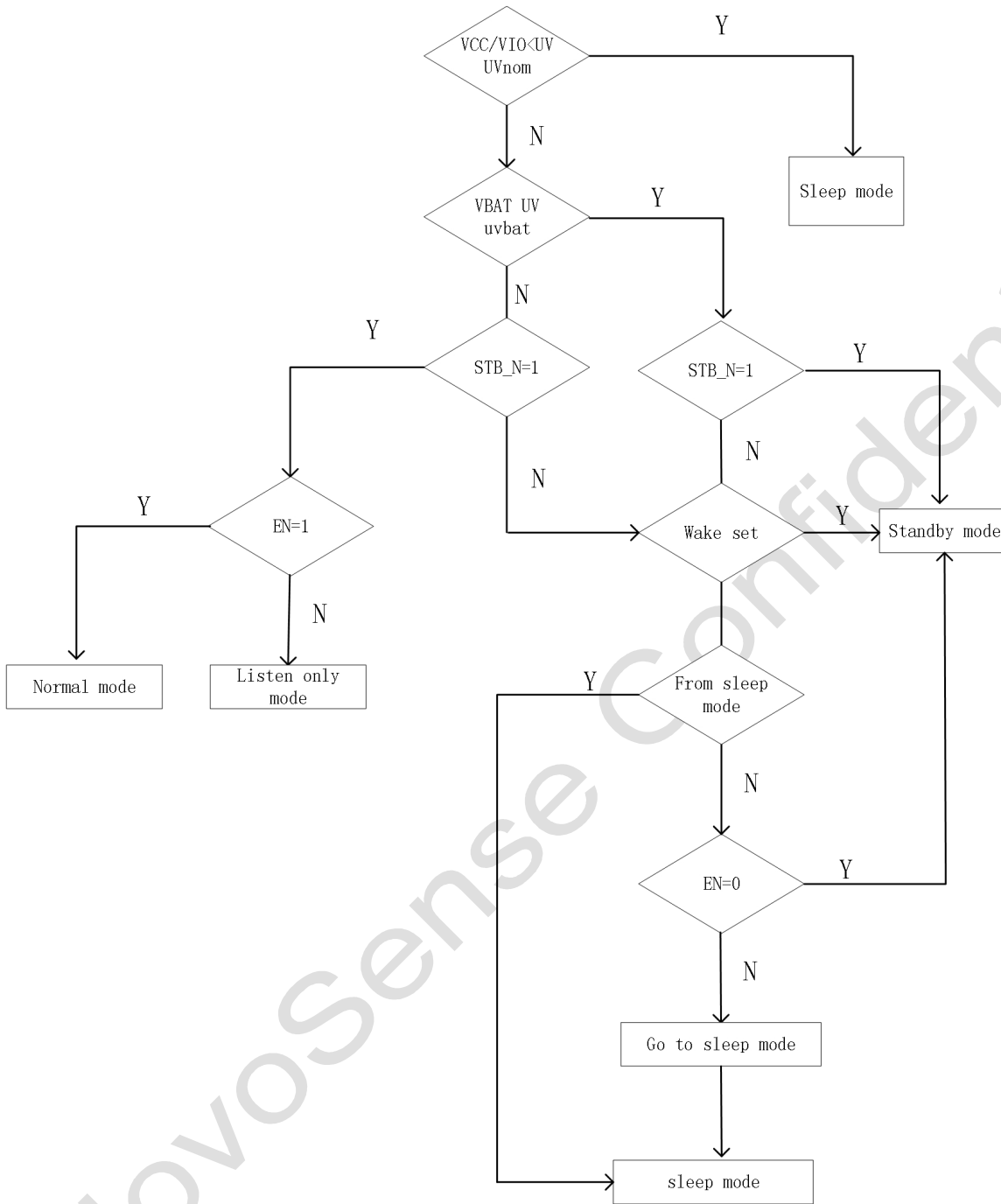
capacitance						
Differential input resistance	R_{ID}	19		80	k Ω	-2 V < V_{CANL} < +7 V; -2V < V_{CANH} < +7 V;
Input resistance	R_{IN}	9	15	40	k Ω	-2 V < V_{CANL} < +7 V; -2V < V_{CANH} < +7 V;
Input resistance matching	$R_{I_{match}}$	-3		+3	%	0 V < V_{CANL} < +5 V; 0V < V_{CANH} < +5 V;
Common-mode voltage range	V_{COM}	-30		+30	V	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Loop delay1	T_{loop1}	60	100	250	ns	Driver input to receiver output, Recessive to Dominant, normal mode
Loop delay2	T_{loop2}	60	100	250	ns	Driver input to receiver output, Dominant to Recessive, normal mode
undervoltage detection time	$T_{del}(uv)$	100		350	ms	
undervoltage recovery time	$T_{rec}(uv)$	1		5	ms	
Bus wake up time	T_{wake}	0.5		5	us	
transmitted recessive bit width	$t_{bit(bus)}$	435		530	ns	$t_{bit(TXD)} = 500$ ns
		155		210	ns	$t_{bit(TXD)} = 200$ ns
bit time on pin RXD	$t_{bit(RXD)}$	400		550	ns	$t_{bit(TXD)} = 500$ ns
		120		220	ns	$t_{bit(TXD)} = 200$ ns
delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$		65	110	ns	Normal mode
delay time from TXD to bus recessive	$t_{d(TXD-busres)}$		65	140	ns	Normal mode
delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$		60	110	ns	Normal or listen only mode
delay time from bus recessive to RXD	$t_{d(busres-RXD)}$		65	140	ns	Normal or listen only mode
Receiver timing symmetry	Δt_{rec}	-65		40	ns	$t_{bit(TXD)} = 500$ ns
		-45		15	ns	$t_{bit(TXD)} = 200$ ns
Bus dominant time-out time	t_{TXD_DTO}	0.4		1.5	ms	$V_{TXD} = 0$ V; Normal mode

Bus dominant time out time	t_{bus_DTO}	0.4		1.5	ms	bus dominant time-out time
hold time	t_h	20		50	us	from issuing go-to-sleep command to entering Sleep mode
bus dominant wake-up time	$t_{wake(busdom)}$	0.5		3	us	Standby or Sleep mode; VBAT = 12 V
bus recessive wake-up time	$t_{wake(busres)}$	0.5		3	us	Standby or Sleep mode; VBAT = 12 V
bus wake-up timeout time	$T_{to(wake)bus}$	0.5		2	ms	bus wake-up filter time
Wakeup time	t_{wake}	5		50	us	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode

6. Function Description

6.1. Overview



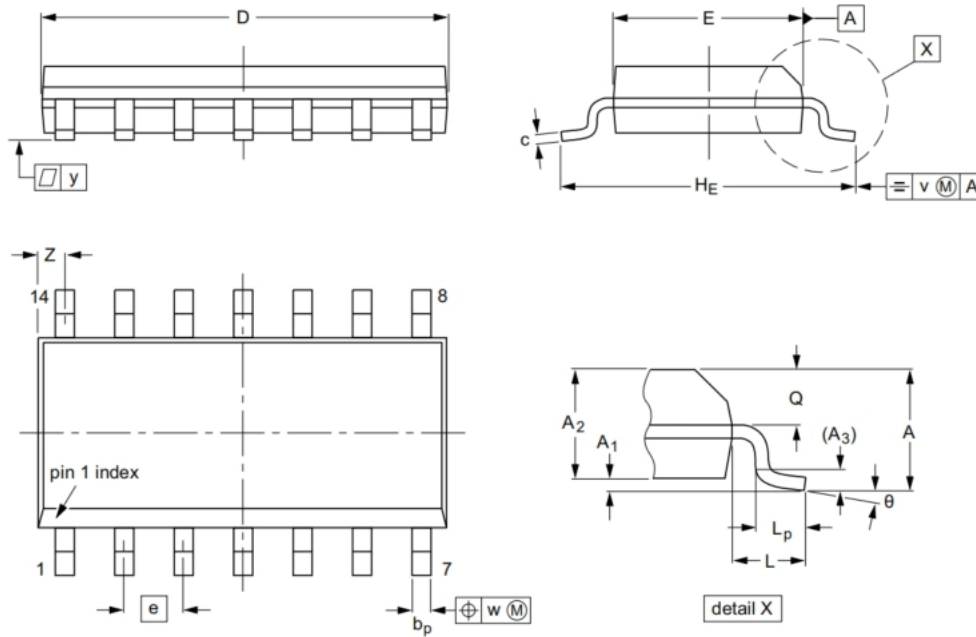
7. Application Note

7.1. Typical Application Circuit

Figure 7.1 Typical PWM isolation circuit for IPM

7.2. PCB Layout

8. Package Information



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Figure 8.1 SOP14 Package Shape and Dimension in millimeters and (inches)

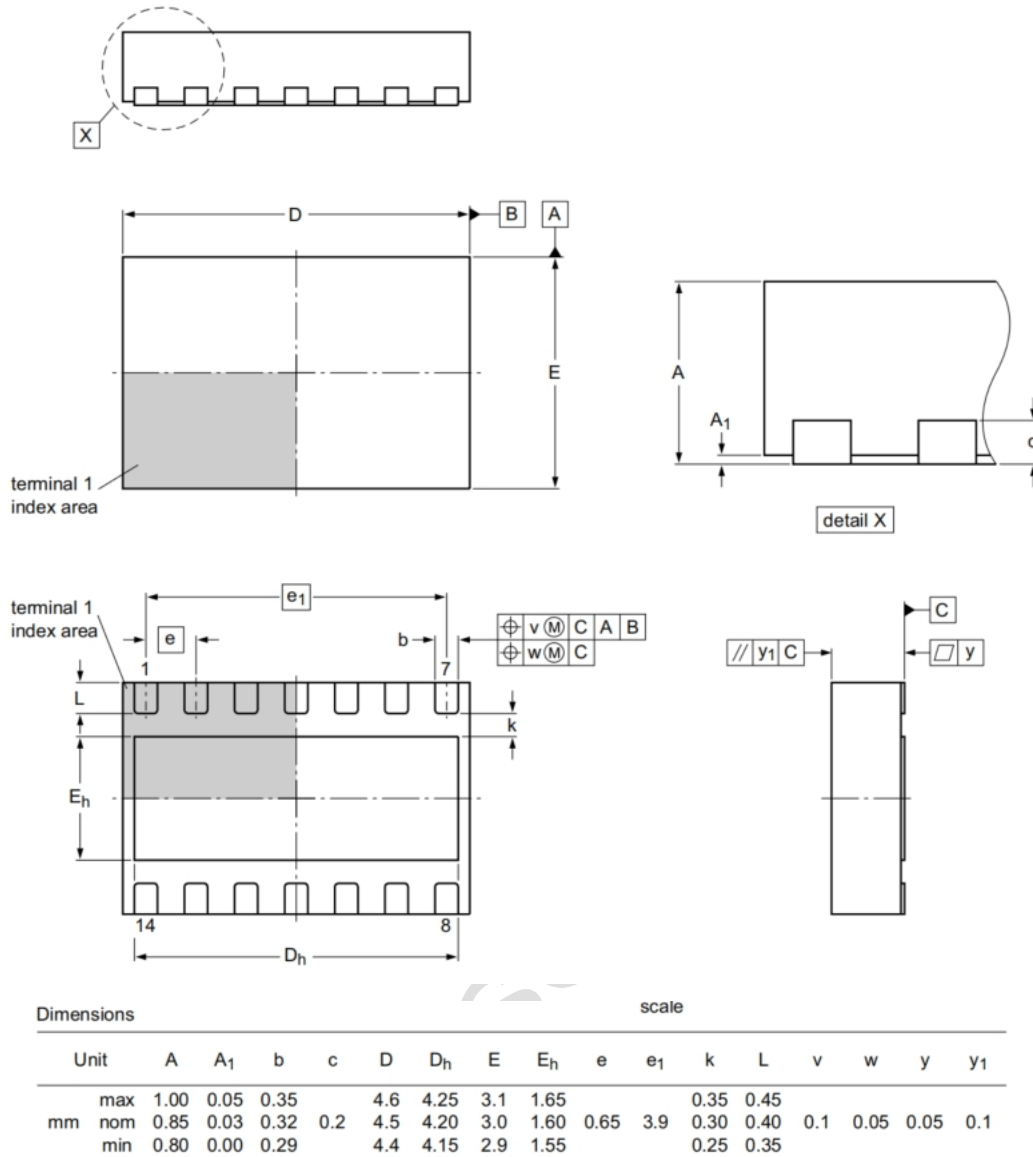


Figure 8.2 DFN14 Package Shape and Dimension in millimeters and (inches)

9. Ordering Information

Part Number	Max Data Rate (Mbps)	Temperature	MSL	Package Type	Package Drawing	SPQ
NCA1043-Q1SPKR	5	-40 to 125°C		SOP14 (150mil)	SOP14	2500
NCA1043-Q1DNKR	5	-40 to 125°C		DFN14	DFN14	

NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

10. Documentation Support

<i>Part Number</i>	<i>Product Folder</i>	<i>Datasheet</i>	<i>Technical Documents</i>	<i>Isolator selection guide</i>
NCA1043	Click here	Click here	Click here	Click here

11. Tape and Reel Information

Figure 12.1 Tape and Reel Information of SOP14

12. Revision History

Revision	Description	Date
0.0	Initial Version	2021/11/20
0.1	changed part number	2022/5/26