NCA1042B-Q1

High-speed CAN Transceiver with Standby Mode

Datasheet (EN) 0.1

Product Overview

The NCA1042B-Q1 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus, which can support at least 110 CAN nodes. The NCA1042B-Q1 implements the CAN physical layer as defined in ISO 11898-2:2016 and SAE J2284-1 to SAE J2284-5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. The NCA1042B-Q1 provides thermal protection and transmit data dominant time out function.

Key Features

- Fully compatible with the ISO11898-2 standard
- I/O voltage range supports 3.3V and 5V MCU
- Power supply voltage
- V_{IO}: 3V to 5.5V
- V_{CC}: 4.5V to 5.5V
- Bus fault protection of -58V to +58V
- Transmit data (TXD) dominant time out function
- Bus dominant time out function in standby mode
- Very low-current Standby mode with wake-up capability
- Over current and over temperature protection
- Date rate: up to 5Mbps
- Low loop delay: <250ns
- Operation temperature: -40℃~125℃
- AEC-Q100 qualified
- RoHS-compliant packages: SOP8, DFN8

Applications

- 5Mbps operation in highly loaded CAN networks down to 10 kbps networks using TXD DTO
- Industrial automation, control, sensors, and drive systems
- Building, security, and climate control automation
- CAN bus standards such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783 and CANaerospace

Device Information

Part Number	Package	Body Size
NCA1042B-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1042B-Q1DNR	DFN8	3.00mm × 3.00mm
NCA1042BN-Q1SPR	SOP8	4.90mm × 3.90mm
NCA1042BN-Q1DNR	DFN8	3.00mm × 3.00mm

Functional Block Diagrams

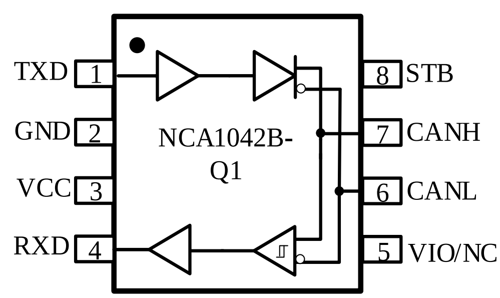

Figure 1. NCA1042B-Q1 Block Diagram

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1. Pin Configuration and Functions

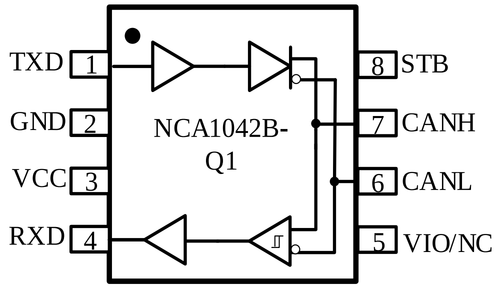


Figure 1-1 NCA1042B-Q1 Package

Table 1-1 NCA1042B-Q1DSPR Pin Configuration and Description

NCA1042B-Q1 PIN NO.	*NCA1042BN-Q1 PIN NO.*	*SYMBOL*	*FUNCTION*
1	1	TXD	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	2	GND	Ground
3	3	VCC	Power Supply
4	4	RXD	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	\	VIO	Logic I/O supply voltage
\	5	NC	No connection
6	6	CANL	Low-level CAN bus line
7	7	CANH	High-level CAN bus line
8	8	STB	STB (standby mode) select pin (active high)

2. Absolute Maximum Ratings

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply Voltage	VCC, VIO	-0.3		7	V	
Logic I/O Voltage	TXD, RXD, STB	-0.3		7	V	
Maximum BUS Pin Voltage	V_{CANH}, V_{CANL}	-58		+58	V	
Voltage between pin CANH and pin CANL	V_{CANH} - V_{CANL}	-20		20	V	
Transient Voltage	V_{trt}	-100			V	On pin CANH and CANL, ISO 7637-2 pulses 1

				75	V	On pin CANH and CANL, ISO 7637-2 pulses 2a
		-150			V	On pin CANH and CANL, ISO 7637-3 pulses 3a
				100	V	On pin CANH and CANL ISO 7637-2 pulses 3b
HBM	ESD	-8		8	kV	CANH and CANL
		-4		4	kV	Other pins
Operating Temperature	T_{opr}	-40		125	℃	
Storage Temperature	T_{stg}	-65		150	℃	

3. Recommended Operating Conditions

Parameters	***Symbol***	***Min***	***Typ***	***Max***	***Unit***
Power Supply Voltage	VCC	4.5	5	5.5	V
I/O Level-Shifting Voltage	VIO	2.8	3.3	5.5	V

4. Thermal Characteristics

Parameters	***Symbol***	***SOP8***	***DFN8***	***Unit***
IC Junction-to-Air Thermal Resistance	$R_{\theta JA}$	145	50	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	50	40	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	45	20	℃/W

5. Specifications

5.1. Electrical Characteristics

V_{CC}=4.5V to 5.5V, V_{IO}=2.8 to 5.5V [1], Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{CC}=5V, V_{IO}=3.3V, Ta = 25℃.

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	Supply voltage		4.5	-	5.5	V
I_{CC}	Supply current	Normal mode, recessive, V_{TXD}=V_{IO}, V_{STB}=0V	2.5	3.5	10	mA
		Normal mode, dominant, V_{TXD} =0V	20	40	70	mA
		Normal mode, dominant, V_{TXD} =0, short circuit on bus lines, -3V < (V_{CANH} = V_{CANL}) <18V	2.5	65	110	mA
		Standby mode, V_{TXD} =V_{IO}	-	1	5	uA
$V_{uvd(VCC)}$	Undervoltage detection voltage on pin VCC	Rising	3.5	3.9	4.5	V
		Falling	3.5	3.8	4.5	V
I/O level adapter supply; pin V_{IO}						
V_{IO}	Supply voltage on pin VIO		2.8	-	5.5	V
I_{IO}	Supply current on pin VIO	Normal mode, recessive, V_{TXD}=V_{IO}	2	22	200	uA
		Normal mode, dominant, V_{TXD}=0V	-	400	1000	uA
		Standby mode; V_{TXD}=V_{IO}	2	11	22	uA
$V_{uvd(VIO)}$	Undervoltage detection voltage on pin VIO	Rising	1.3	2.45	2.7	V
		Falling	1.3	2.35	2.7	V
Standby mode control input; pin STB						
V_{IH}	High level input voltage		0.7*V_{IO}	-	V_{IO}+0.3	V
V_{IL}	Low level input voltage		-0.3	-	0.3*V_{IO}	V
I_{IH}	High level input current	V_{STB}=V_{IO}	-1	-	1	uA
I_{IL}	Low level input current	V_{STB}=0V	-15	-4	-1	uA
CAN transmit data input; pin TXD						
V_{IH}	High level input voltage		0.7*V_{IO}	-	V_{IO}+0.3	V
V_{IL}	Low level input voltage		-0.3	-	0.3*V_{IO}	V
I_{IH}	High level input current	V_{TXD}=V_{IO}	-5	-	5	uA

I_{IL}	Low level input current	V_{TXD}=0V	-260	-90	-30	uA
C_i	Input capacitance	[2]	-	5	10	pF
CAN receive data output; pin RXD						
I_{OH}	High level output current	$V_{RXD} = V_{IO}$ - 0.4V	-8	-3.5	-1	mA
I_{OL}	Low level output current	V_{RXD} = 0.4V; bus dominant	2	4	12	mA
Bus lines; pins CANH and CANL; Driver						
$V_{OH(D)}$	CANH output voltage (Dominant)	V_{TXD} =0V, R_L=50Ω to 65Ω	2.75	3.7	4.5	V
$V_{OL(D)}$	CANL output voltage (Dominant)	V_{TXD} =0V, R_L=50Ω to 65Ω	0.5	1.2	2.25	V
$V_{O(R)}$	CANH or CANL output voltage (Recessive)	Normal mode, no load	2	0.5*V_{CC}	3	V
		Standby mode, no load	-0.1	-	0.1	V
$V_{OD(D)}$	Differential output voltage (Dominant)	Normal mode				
		R_L = 45Ω to 65Ω	1.5	-	3	V
		R_L = 45Ω to 70Ω	1.5	-	3.3	V
		R_L = 2240Ω	1.5	-	5	V
$V_{OD(R)}$	Differential output voltage (Recessive)	Normal mode, no load	-50	-	50	mV
		Standby mode, no Load	-0.2	-	0.2	V
$I_{OSH(R)}$	CANH short-circuit output current, recessive	Normal mode, $V_{CANH} = V_{CANL}$ = -27V to 32V	-115	-	115	mA
$I_{OSL(R)}$	CANL short-circuit output current, recessive	Normal mode, $V_{CANH} = V_{CANL}$ = -27V to 32V	-115	-	115	mA
$I_{OSH(D)}$	CANH short-circuit output current, dominant	Normal mode, V_{CANH} = -15V to 40V, CANL open	-115	-70	115	mA
$I_{OSL(D)}$	CANL short-circuit output current, dominant	Normal mode, V_{CANL} = -15V to 40V, CANH open	-115	70	115	mA
Bus lines; pins CANH and CANL; Receiver						
$V_{ID(R)}$	Differential input threshold voltage, recessive	-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V				
		Normal mode	0.5	0.7	0.9	V
		-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V				
		Standby mode	0.4	0.65	1.15	V
$V_{ID(D)}$		-12V < V_{CANH} < 12V, -12V < V_{CANL} < 12V				

	Differential input threshold voltage, dominant	Normal mode	0.5	0.8	0.9	V
		$-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$				
		Standby mode	0.4	0.65	1.15	V
V_{hys}	Differential input hysteresis voltage	$-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$	50	80	200	mV
$V_{RX(R)}$	Receiver recessive voltage	$-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$				
		Normal mode	-4	-	0.5	V
		$-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$				
		Standby mode	-4	-	0.4	V
$V_{RX(D)}$	Receiver dominant voltage	$-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$				
		Normal mode	0.9	-	9	V
		$-12V < V_{CANH} < 12V$, $-12V < V_{CANL} < 12V$				
		Standby mode	1.15	-	9	V
$I_{LKG(OFF)}$	Power-off (unpowered) bus input leakage current	$V_{CANH} = V_{CANL} = 5V$, $V_{CC} = V_{IO} = 0V$	-5	-	5	uA
R_{IN}	Input resistance	$-2V \le V_{CANH} \le 7V$, $-2V \le V_{CANL} \le 7V$ [2]	9	15	28	kΩ
RI_{match}	Input resistance matching	$V_{CANH} = 5V$, $V_{CANL} = 5V$, $RI_{match}=2*(R_{CANH}-R_{CANL})/(R_{CANH}+R_{CANL})$ [2]	-1	-	1	%
R_{ID}	Differential input resistance	$-2V \le V_{CANH} \le 7V$, $-2V \le V_{CANL} \le 7V$, $R_{ID}=R_{CANH}+R_{CANL}$ [2]	19	31	52	kΩ
C_I	Input capacitance to ground	CANH or CANL [2]	-	13	-	pF
C_{ID}	Differential input	[2]	-	5	-	pF
Temperature detection						
T_{SD}	Thermal shutdown threshold	[2]	-	193	-	℃
$T_{SD(hys)}$	Thermal shutdown hysteresis	[2]	-	11	-	℃

[1] Only NCA1042B has a VIO pin. For NCA1042BN, the VIO input is internally connected to VCC.

[2] Not tested in production; guaranteed by design.

5.2. Switching Electrical Characteristics

V_{CC} =4.5V~5.5V, V_{IO}=2.8~5.5V,Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Ta = 25℃

Symbol	Parameters	Comments	Min	Typ	Max	Unit
Driver						
$t_{d(TXD-bus, dom)}$	Delay time from TXD to bus dominant	Normal mode	-	45	-	ns
$t_{d(TXD-bus, rec)}$	Delay time from TXD to bus recessive	Normal mode	-	50	-	ns
$t_{r(bus)}$	Differential output signal rise time		-	45	-	ns
$t_{f(bus)}$	Differential output signal fall time		-	30	-	ns
$t_{bit(bus)}$	Transmitted recessive bit width	$t_{bit(TXD)}$ = 500 ns	435	500	530	ns
		$t_{bit(TXD)}$ = 200 ns	155	190	210	ns
t_{TXD_DTO}	Bus dominant time-out time		800	1350	10000	us
Receiver						
$t_{d(bus-RXD, dom)}$	Delay time from bus to RXD dominant		-	70	-	ns
$t_{d(bus-RXD, rec)}$	Delay time from bus to RXD recessive		-	90	-	ns
$t_{d(TXD-RXD, dom)}$	Delay time from TXD to RXD dominant	Normal mode	-	110	220	ns
$t_{d(TXD-RXD, rec)}$	Delay time from TXD to RXD recessive	Normal mode	-	140	220	ns
$t_{r(RXD)}$	RXD signal rise time		-	5	-	ns
$t_{f(RXD)}$	RXD signal fall time		-	5	-	ns
$t_{bit(RXD)}$	Bit time on pin RXD	$t_{bit(TXD)}$ = 500 ns	400	470	550	ns
		$t_{bit(TXD)}$ = 200 ns	120	170	220	ns
Δt_{rec}	Receiver timing symmetry	Distortion of RXD relative to bus				
		$t_{bit(TXD)}$ = 500 ns	-65	-35	40	ns
		$t_{bit(TXD)}$ = 200 ns	-45	-20	15	ns
t_{bus_DTO}	Bus dominant time out	Standby mode	800	1350	10000	us
$t_{fltr(wake)bus}$	Bus wake-up filter time	Standby mode, VIO version	0.5	1.5	5	us
		Standby mode, SPLIT version	0.5	1.5	5	us

$t_{d(stb\text{-}norm)}$	Standby to normal mode delay time				47	us

5.3. Parameter Measurement Information

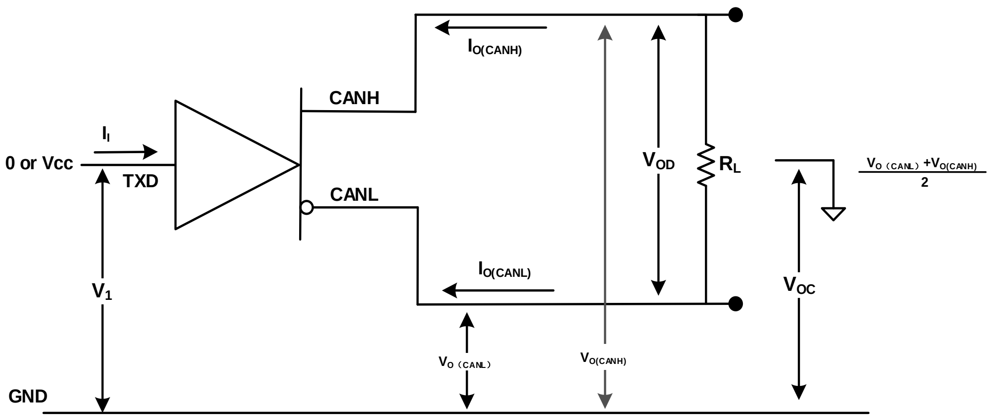


Figure 5-1 Driver Voltage, Current and Test Definitions

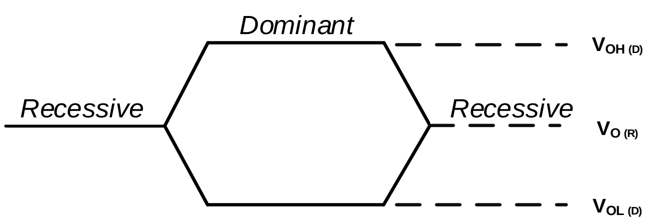
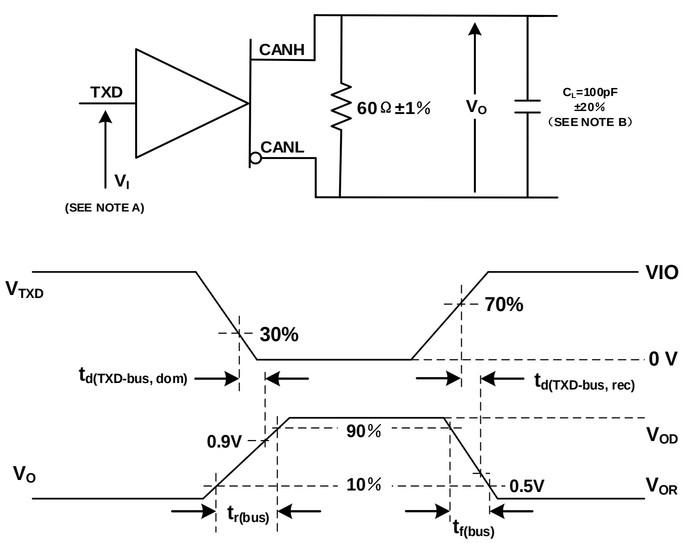


Figure 5-2 Bus Logic State Voltage Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5-3 Driver Test Circuit and Voltage Waveforms

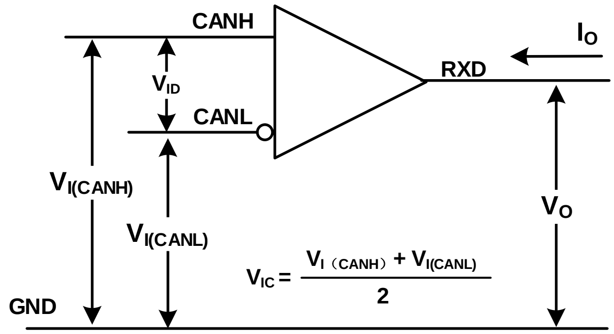
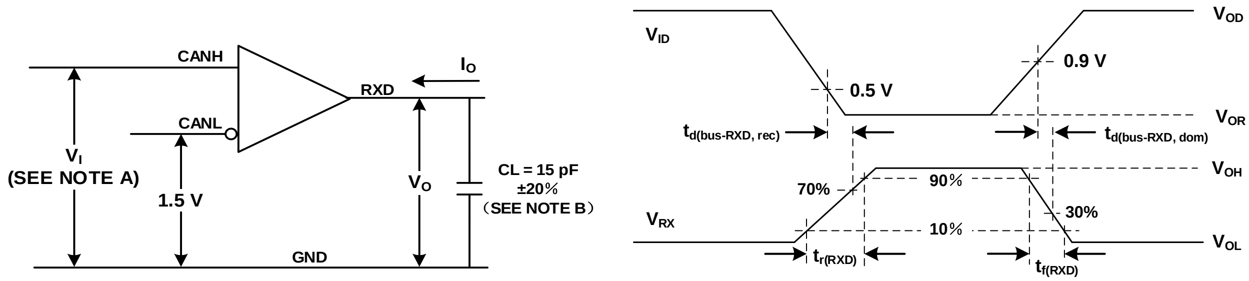


Figure 5-4 Receiver Voltage and Current Definitions



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5-5 Receiver Test Circuit and Voltage Waveforms

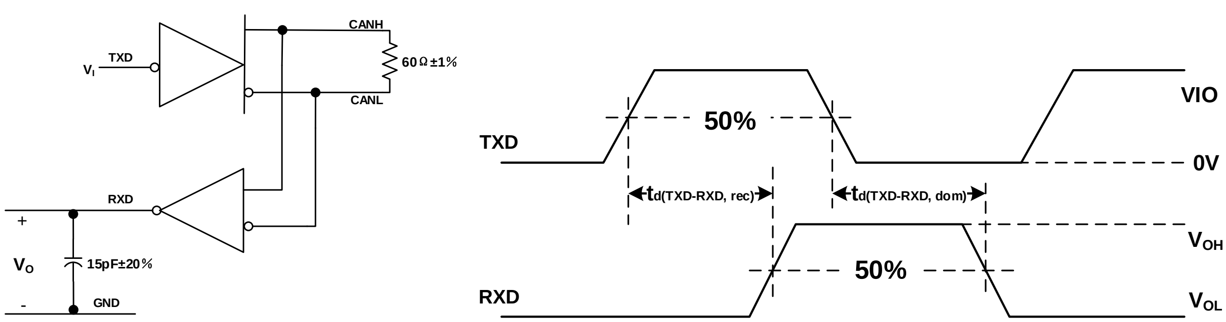
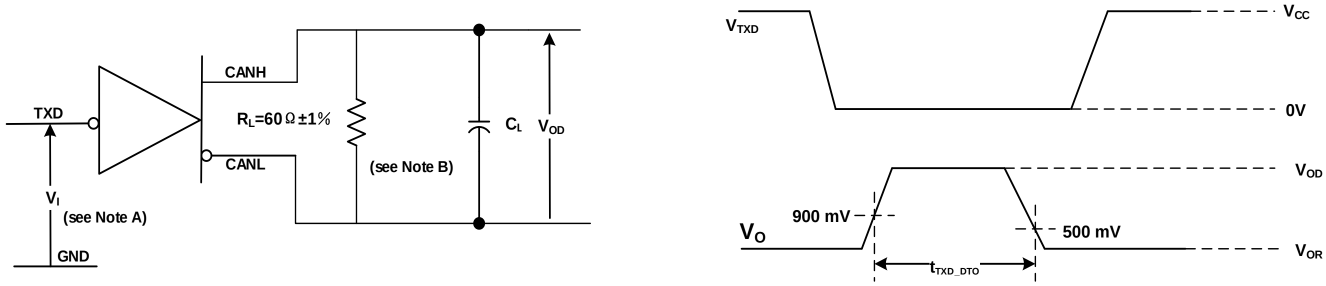


Figure 5-6 t_{loop} Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r \le 6$ ns, $t_f \le 6$ ns, $Z_O = 50\ \Omega$.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 5-7 Dominant Time-out Test Circuit and Voltage Waveforms

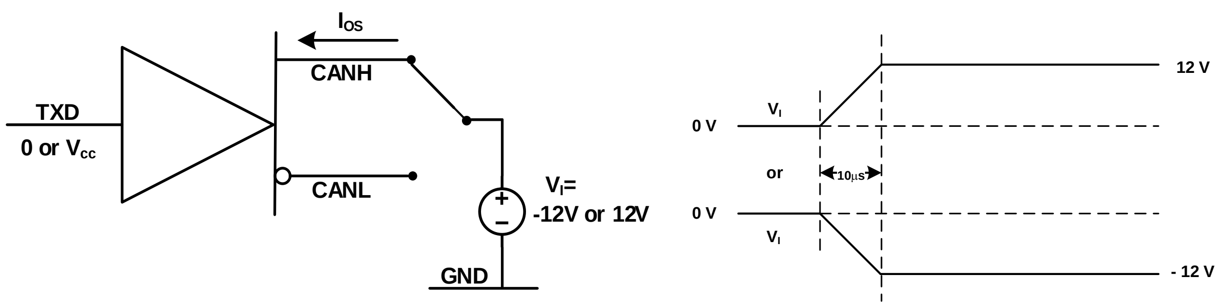


Figure 5-8 Driver Short-Circuit Current Test Circuit and Waveforms

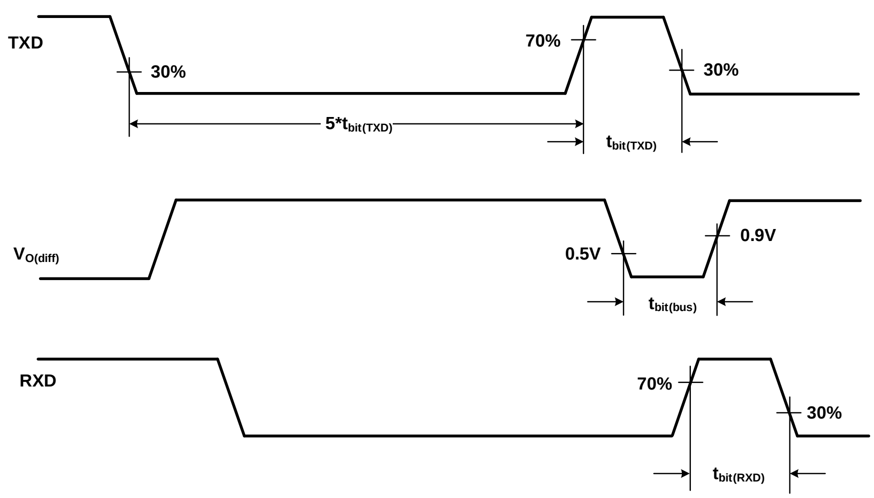


Figure 5-9 $t_{bit(RXD)}$ Test Circuit and Waveforms

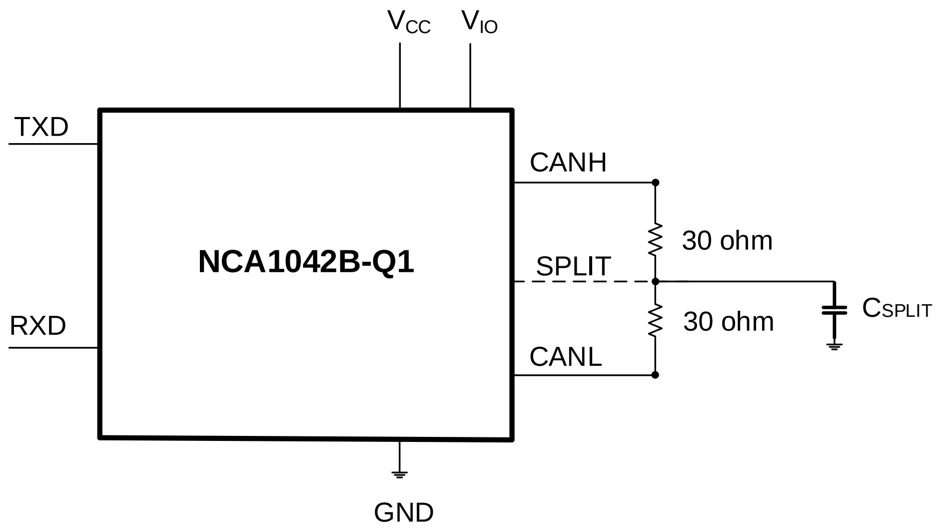


Figure 5-3 Test circuit for measuring transceiver driver symmetry

5.4. Typical Characteristics

V_{CC} =4.5V~5.5V, V_{IO}=2.8~5.5V, R_L=45~70 ohm, Ta=-40℃ to 125℃. Unless otherwise noted, Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, R_L=60 ohm, Ta = 25℃.

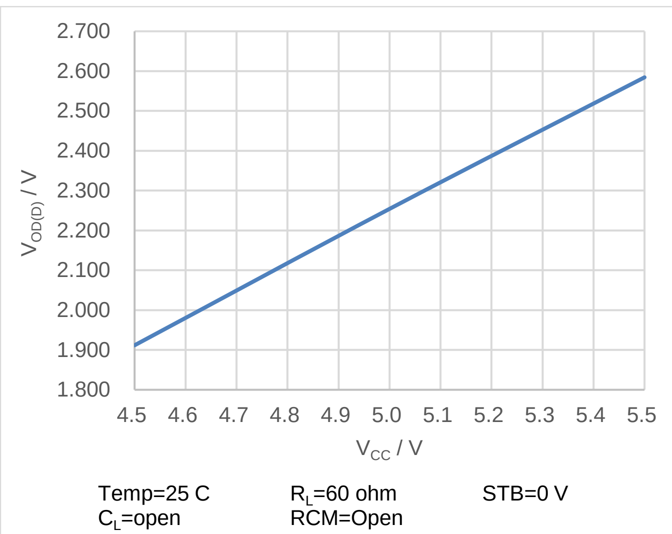


Figure 5-4 $V_{OD(D)}$ vs VCC

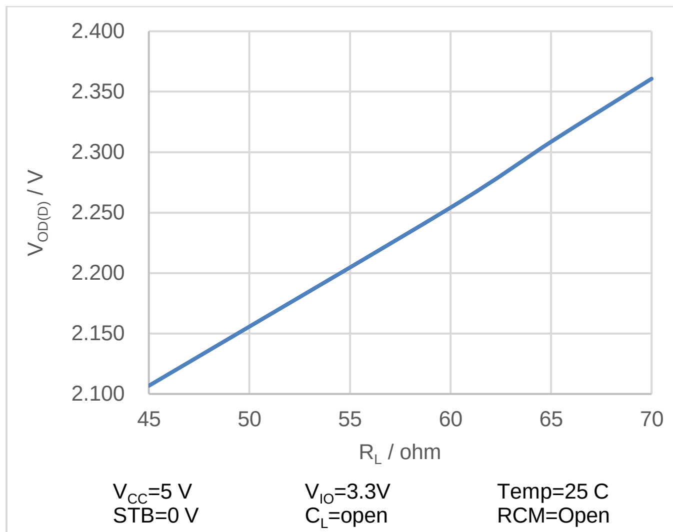


Figure 5-5 $V_{OD(D)}$ vs R_L

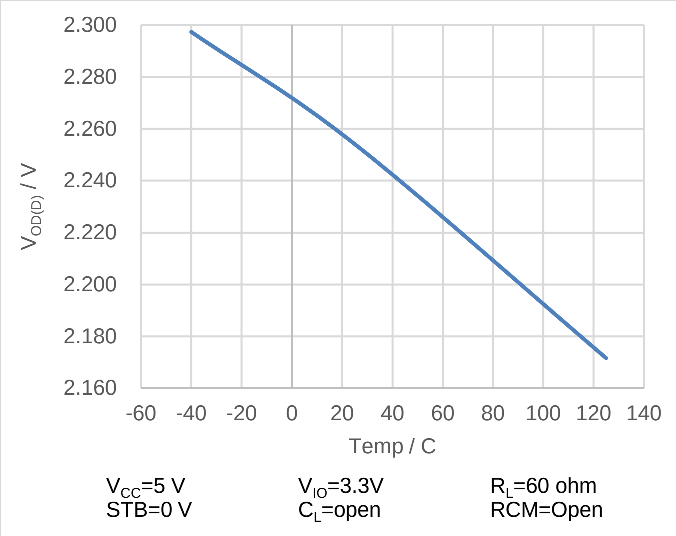


Figure 5-6 $V_{OD(D)}$ vs Temperature

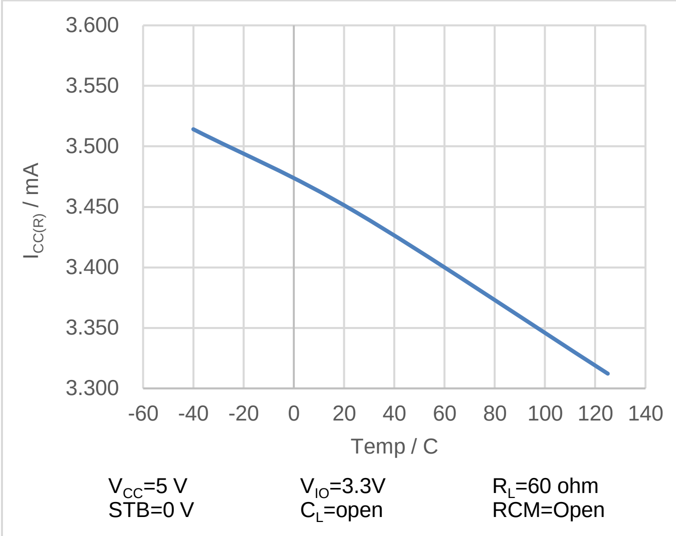


Figure 5-7 $I_{CC(R)}$ vs Temperature

6. Function Description

6.1. Overview

The NCA1042B-Q1 is a CAN transceiver which fully compatible with the ISO11898-2 standard. The NCA1042B-Q1 is providing high electromagnetic immunity and low emissions. The data rate of the NCA1042B-Q1 is up to 5Mbps, and it can support at least 110 CAN nodes. The NCA1042B-Q1 provides thermal protection and transmit data dominant time out function.

6.2. Functional Block Diagram

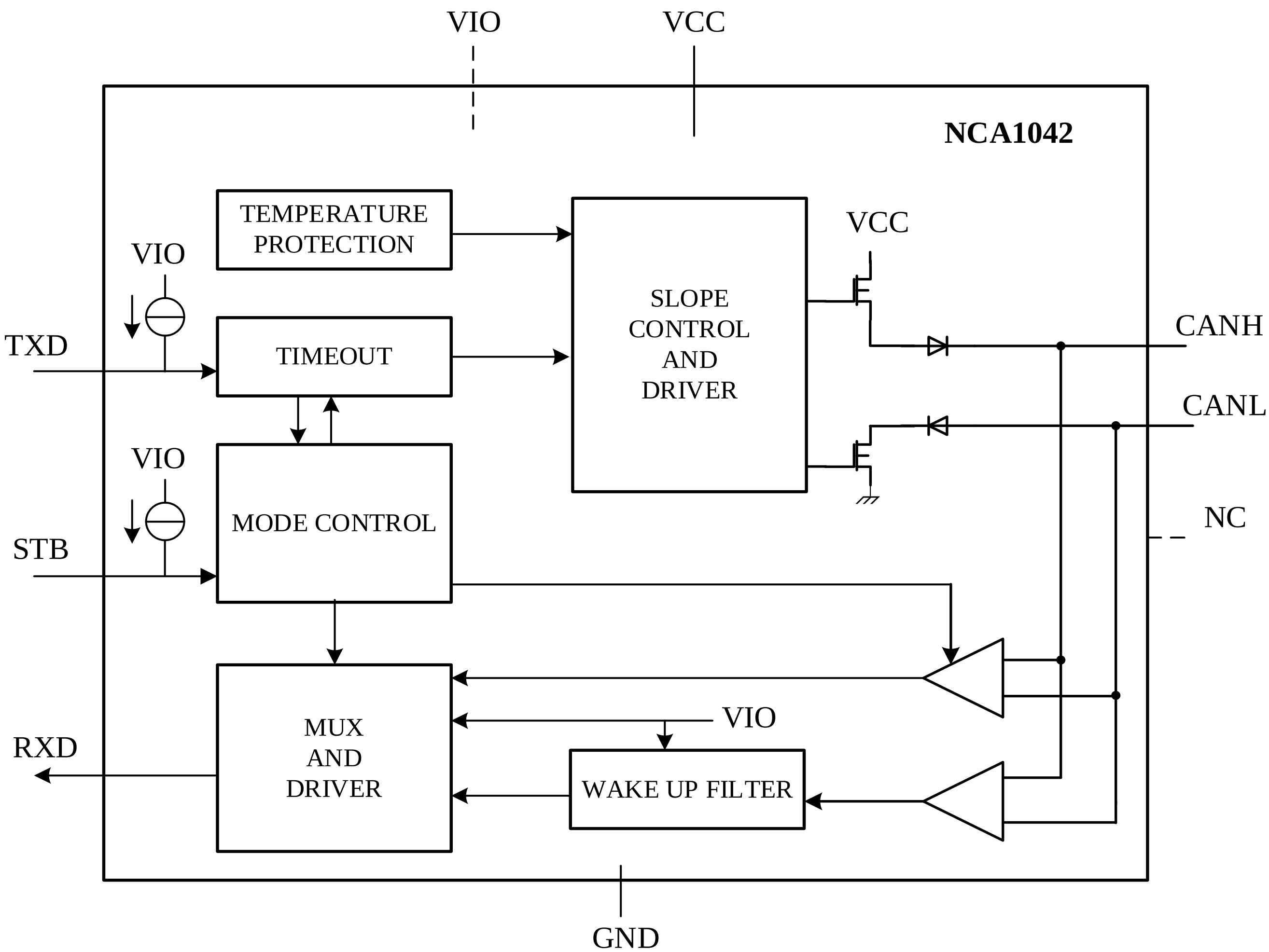


Figure 6-1 Block diagram of NCA1042B-Q1

6.3. Feature Description

6.3.1. TXD Dominant Time-Out Function (TXD DTO)

A 'TXD dominant time-out' timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{TXD_DTO}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD. The TXD dominant time-out time also defines the minimum possible bit rate of 10 kbit/s.

6.3.2. Bus Dominant Time-Out Function (Bus DTO)

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than t_{bus_DTO}, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

6.3.3. Undervoltage Detection on Pins VCC and VIO

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the VCC or VIO supply terminals. When VCC drop below the VCC undervoltage detection level, $V_{uvd(VCC)}$, the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered. When VIO drop below the VIO undervoltage detection level, $V_{uvd(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until VIO has recovered.

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation within 50 µs.

Table 6-1 Undervoltage Lockout 5V Only Devices (NCA1042BN)

VCC	Device State	Bus Output	RXD
>UV_{VCC}	Normal	Per TXD	Mirrors Bus[1]
<UV_{VCC}	Protected	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

Table 6-2 Undervoltage Lockout I/O Level Shifting Devices (NCA1042B)

VCC	VIO	Device State	Bus Output	RXD
>UV_{VCC}	>UV_{VIO}	Normal	Per TXD	Mirrors Bus[1]
<UV_{VCC}	>UV_{VIO}	STB=HIGH: Standby Mode	Recessive	Bus Wake RXD Request
		STB=LOW: Protected Mode	High Impedance	High (Recessive)
>UV_{VCC}	<UV_{VIO}	Protected	High Impedance	High Impedance
<UV_{VCC}	<UV_{VIO}	Protected	High Impedance	High Impedance

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

6.3.4. Unpowered Device

The device is designed to be 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

6.3.5. Internal Biasing of TXD and STB Input Pins

Pins TXD and STB have internal pull-ups to VIO to ensure a safe, defined state, in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

6.3.6. Over-Temperature Protection (OTP)

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature T_{SD}, the output drivers will be disabled until the virtual junction temperature becomes lower than T_{SD} and TXD becomes recessive again. By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

6.3.7.Over-Current Protec tion (OCP)

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

6.3.8.VIO Supply Pin

Pin VIO should be connected to the microcontroller supply voltage (see Figure 7-2). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin VIO also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC.

For versions of the NCA1042BN without a VIO pin, the VIO input is internally connected to VCC. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 5 V microcontrollers.

6.4. Device Functional Modes

The device has two main operating modes: Normal mode and Standby mode. Operating mode is selected via the STB input pin.

Table 6-3 Operating Modes

STB	Mode	Driver	Receiver	RXD Terminal
L	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State[1]
H	Standby Mode	Disabled (OFF)	Disabled (OFF) (Low Power Bus Monitor is Active)	High (Unless valid WUP has been received)

[1] Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

6.4.1.CAN Bus States

The CAN bus has two states during powered operation: dominant and recessive. A dominant bus state is when the bus is driven differentially, corresponding to a logic LOW on the TXD and RXD terminal. A recessive bus state is when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic HIGH on the TXD and RXD terminals.

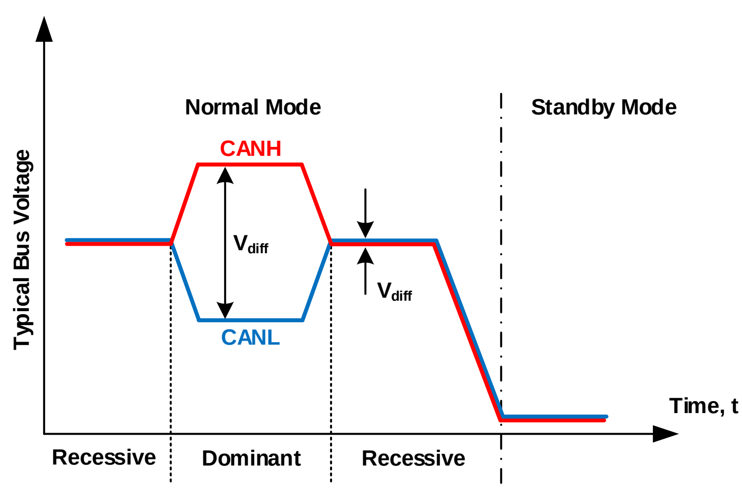


Figure 6-2 Bus States

6.4.2.Normal Mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 6-1). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

6.4.3.Standby Mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)}$ bus are reflected on pin RXD.

In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by V_{IO}, and is capable of detecting CAN bus activity even if V_{IO} is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

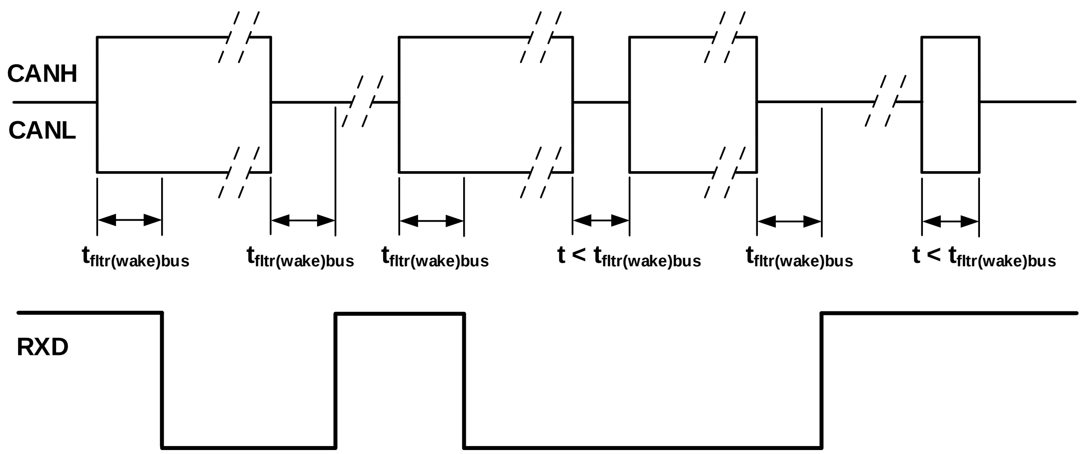


Figure 6-3 Wake-Up Timing

6.4.4.Driver and Receiver Function Tables

Table 6-4 Driver Function Table

Inputs		Outputs		Driven Bus State
STB[1]	TXD[1 2]	CANH[1]	CANL[1]	
L	L	H	L	Dominant
	H or Open	Z	Z	Recessive
H or Open	X	Z	Z	Recessive

[1] H= high level; L=low level; X=irrelevant; Z= common mode(recessive) bias to $V_{CC}/2$.

[2] Devices have an internal pull up to VCC or VIO on TXD terminal. If the TXD terminal is open, the terminal is pulled HIGH and the transmitter remain in recessive (non-driven) state.

Table 6-5 Receiver Function Table

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Terminal
Normal	$V_{ID} \geq V_{ID(D)}$	Dominant	L
	$V_{ID(R)} < V_{ID} < V_{ID(D)}$	Uncertain	Uncertain
	$V_{ID} \leq V_{ID(R)}$	Recessive	H
	Open	Recessive	H

[1] H= high level; L=low level.

7. Application Information

7.1. Typical Application

The NCA1042B-Q1 requires a 0.1 µF bypass capacitors between VCC and GND. The capacitor should be placed as close as possible to the package. The Figure 7-1 and Figure 7-2 are the typical applications of NCA1042B-Q1.

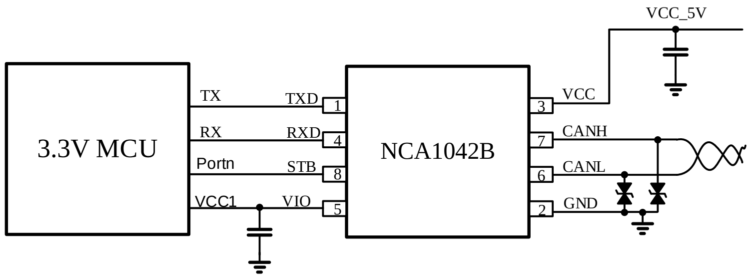


Figure 7-1 Typical CAN Bus Application Using 3.3V CAN Controller

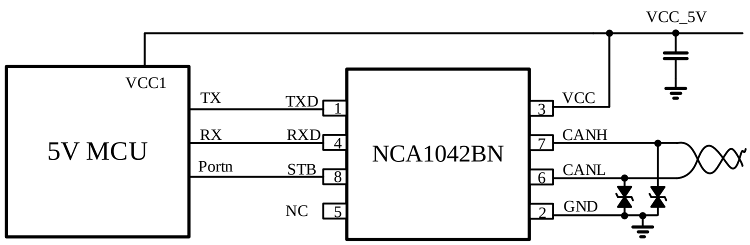
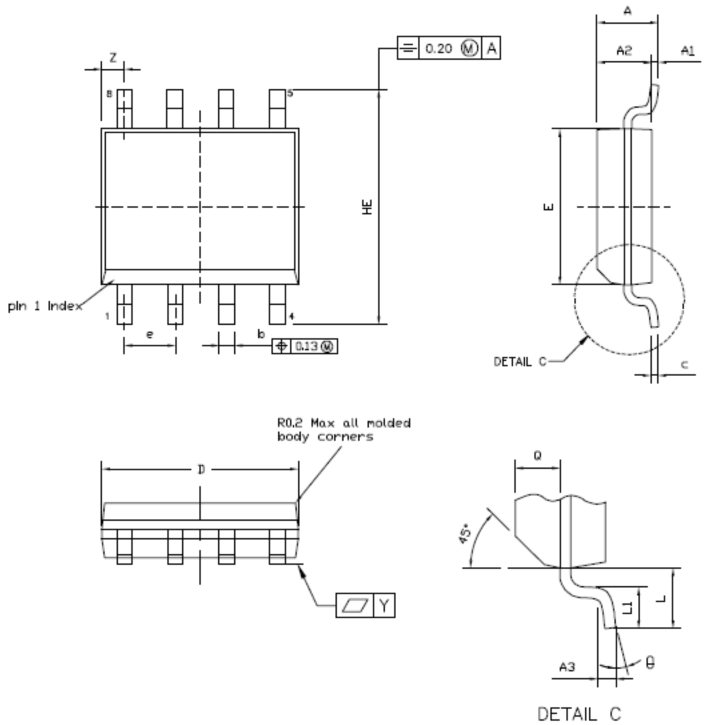


Figure 7-2 Typical CAN Bus Application Using 5V CAN Controller

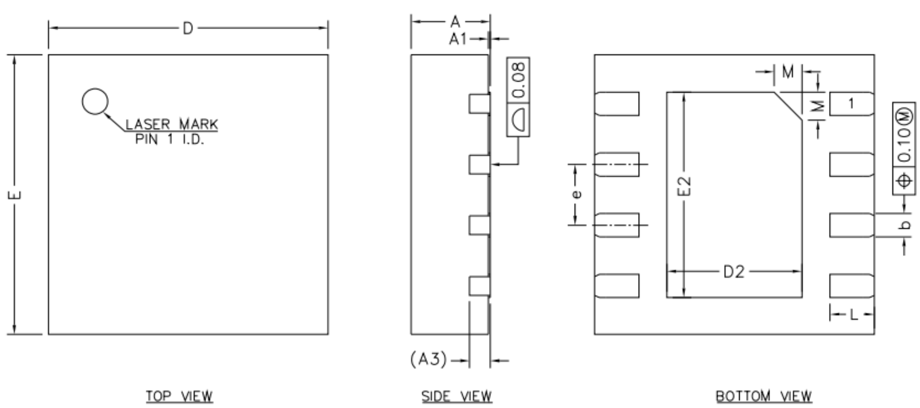
8. Package Information



✱ CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 8-1 SOP8 Package Shape and Dimension in millimeters (inches)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203REF		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	1.35	1.45	1.60
E2	2.10	2.20	2.35
e	0.55	0.65	0.75
L	0.425	0.475	0.525
M	0.30REF		

Figure 8-2 DFN8 Package Shape and Dimension in millimeters (inches)

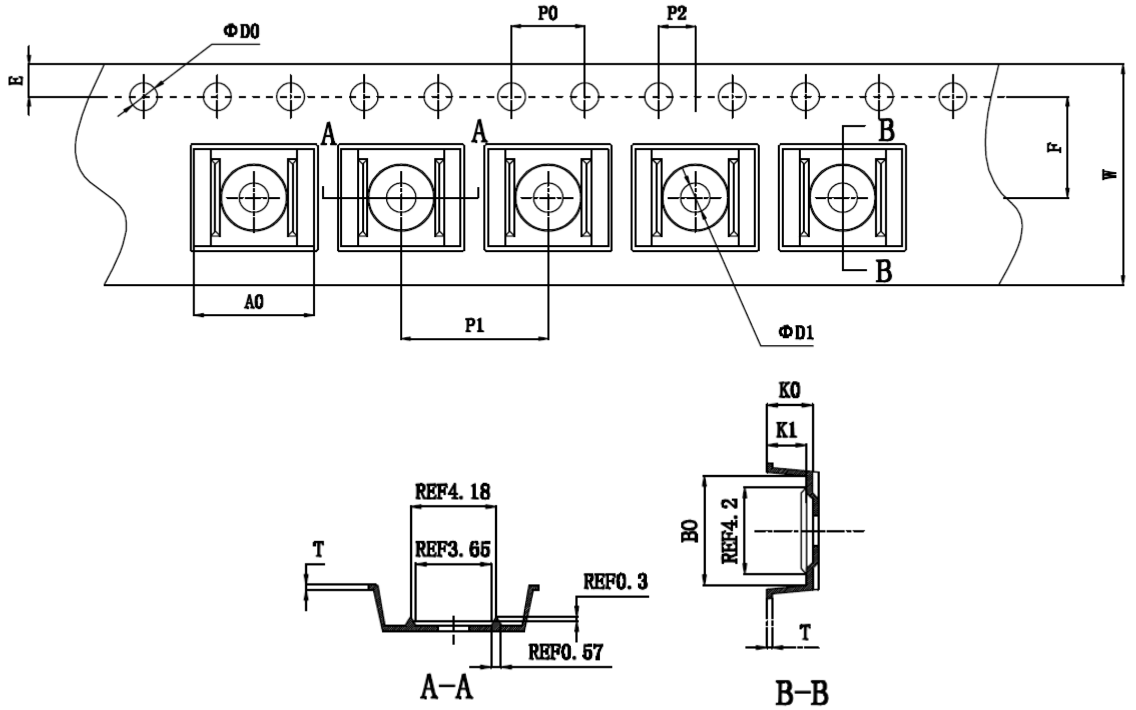
9. Order Information

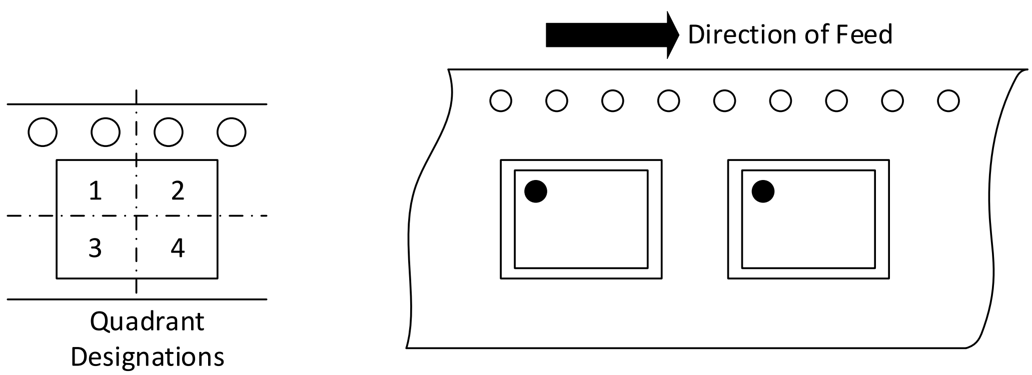
Part Number	*Max Data Rate (Mbps)*	*Operation Temperature*	*MSL*	*Package Type*	*Package Drawing*	*SPQ*
NCA1042B-Q1SPR	5	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NCA1042B-Q1DNR	5	-40 to 125℃	1	DFN8	DFN8	3000
NCA1042BN-Q1SPR	5	-40 to 125℃	1	SOP8 (150mil)	SOP8	2500
NCA1042BN-Q1DNR	5	-40 to 125℃	1	DFN8	DFN8	3000
NOTE: All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.						

10. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator Selection Guide*
NCA1042B-Q1	Click here	Click here	Click here	Click here

11. Tape and Reel Information





Parameter	Dimension (mm)
E	1.75±0.10
F	5.5±0.10
P2	2.00±0.10
D0	1.55±0.05
D1	1.6±0.10
P0	4.00±0.10
10P0	40.00±0.20

Parameter	Dimension (mm)
W	12.00±0.30
P1	8.00±0.10
A0	6.50±0.10
B0	5.30±0.10
K0	2.20±0.10
K1	1.90±0.10
T	0.30±0.05

Figure 11-1 Tape and Reel Information of SOP8

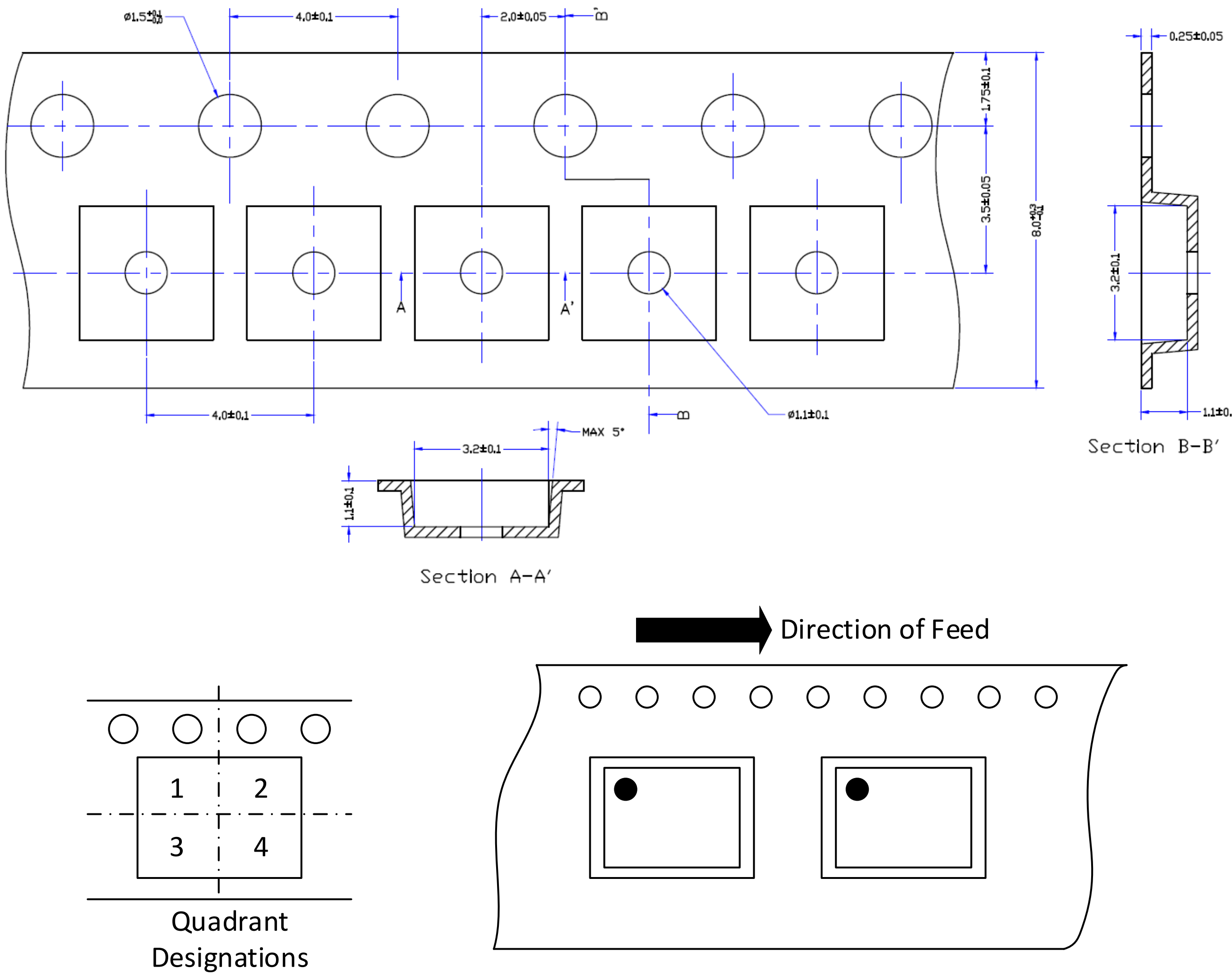


Figure 11-2 Tape and Reel Information of DFN8

12. Revision History

Revision	Description	Date
0.0	Initial version	2022/12/1
0.1	Updated spec value	2023/1/18

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