# M1505 Hardware Design

**Smart Module Series**

**Version：** V1.2

**Date：** 2016-10-30

Shanghai Mobiletek Communication Ltd

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# Version History

| Date | Version | Description of change | Author |
|---|---|---|---|
| 2016-07-06 | V1.0 | Initial version | Rc.dong |
| 2016-08-08 | V1.1 | Modify the PIN Name | Rc.dong |
| 2016-10-30 | V1.2 | Modify the format | Rc.dong |
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# 1. Overview

M1505 is a WIFI module with SMT package. For the stable performance, the compact appearance, high cost-performance ratio and good extensibility, it can be applied to a variety of compact product designs. Products are mainly targeted at users without requiring communication smart SOM（System on Module）.

## 1.1 System Block Diagram

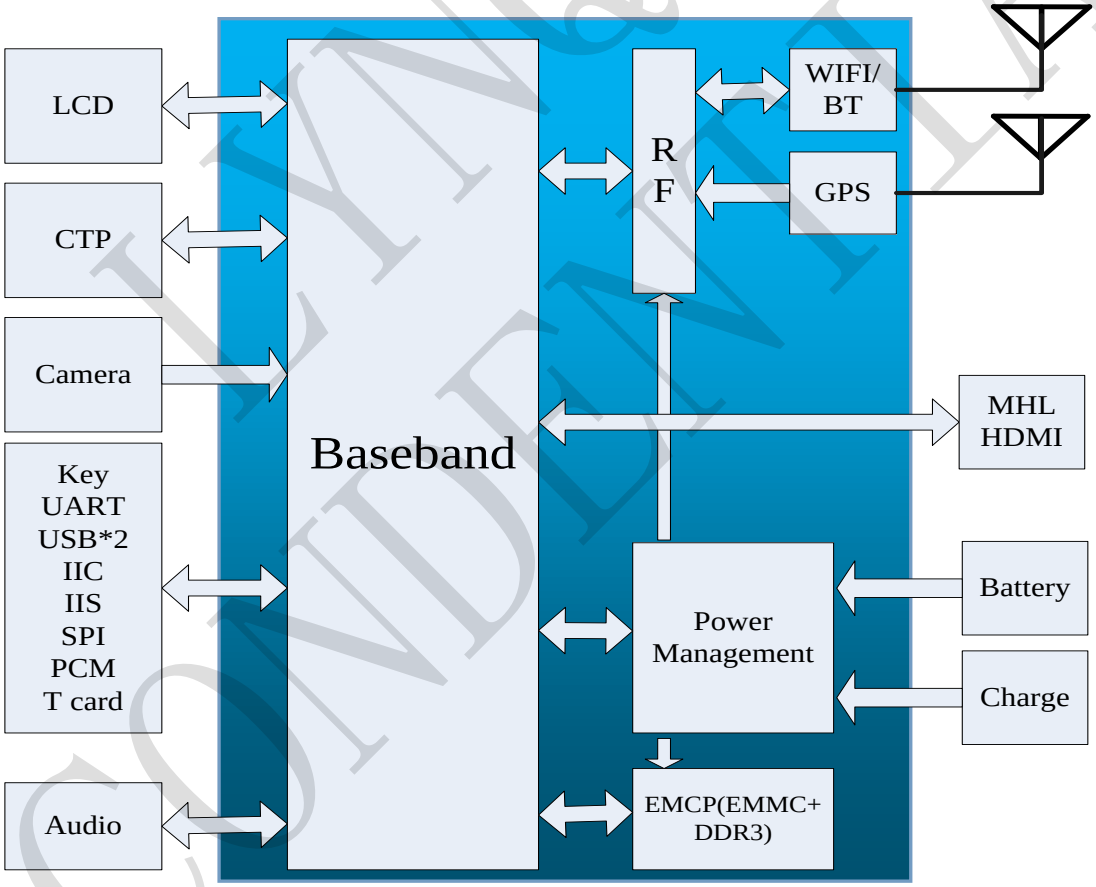


Figure 1-1 M1505 functional diagram

## 1.2 Features

- Operating System

  Android 5.1 (64bit)

- Processor

  Quad-core ARM@Cortex-A53 1.3GHz

- Memory

  8GB eMMC+8Gb LPDDR3

- Graphics

  Mali-T720 MP2 @520MHz and 115Mtri/s, 1.0Gpix/s

- Video

  Decode：H.264 1080P@30fps/40Mbps
  Encode：H.264 1080P@30fps

- Audio

  Sampling rates: 8kHz to 192kHz
  Sampling formats: 16/24-bit, Mono/Stereo

- Wireless connection

  WIFI: Support 802.11 a/b/g/n
  FM: FM Receiver
  Bluetooth: BT3.0/4.0
  GPS: GPS

- Sensor

  Support 12 bit tri-axis accelerometer

- User Interface

  LCM：FWXGA 1366x768 60fps
  TP：Capacitive touch panel
  Audio：3 differential MIC inputs, 1 output
  Front camera：5MP

Rear camera：13MP

## 1.3 Specifications

- Supply voltage range：3.50V to 4.35V
- Size：46.0mm X 35.0mm X 2.80mm
- 135-pin LCC
- Operating Temperature：-30℃ to +75℃
- Storage temperature range：-40℃ to +85℃
- 2 antenna（ WIFI/BT、GPS ）

## 1.4 Interface

- SPI
- GPIO
- EINT
- 4 UART
- 2 IIC
- Key
- IIS
- LCD（MIPI DSI/LVDS）
- TF card
- 2 Camera(MIPI CSI)
- USB HUB
- USB 2.0 HS peripheral (OTG)



 

- Charge

## 1.5 Application Prospect

- HD video monitor
- Automation control devices
- Home Care devices
- POS

# 2. Module Pin Definitions

## 2.1 Pin Distribution

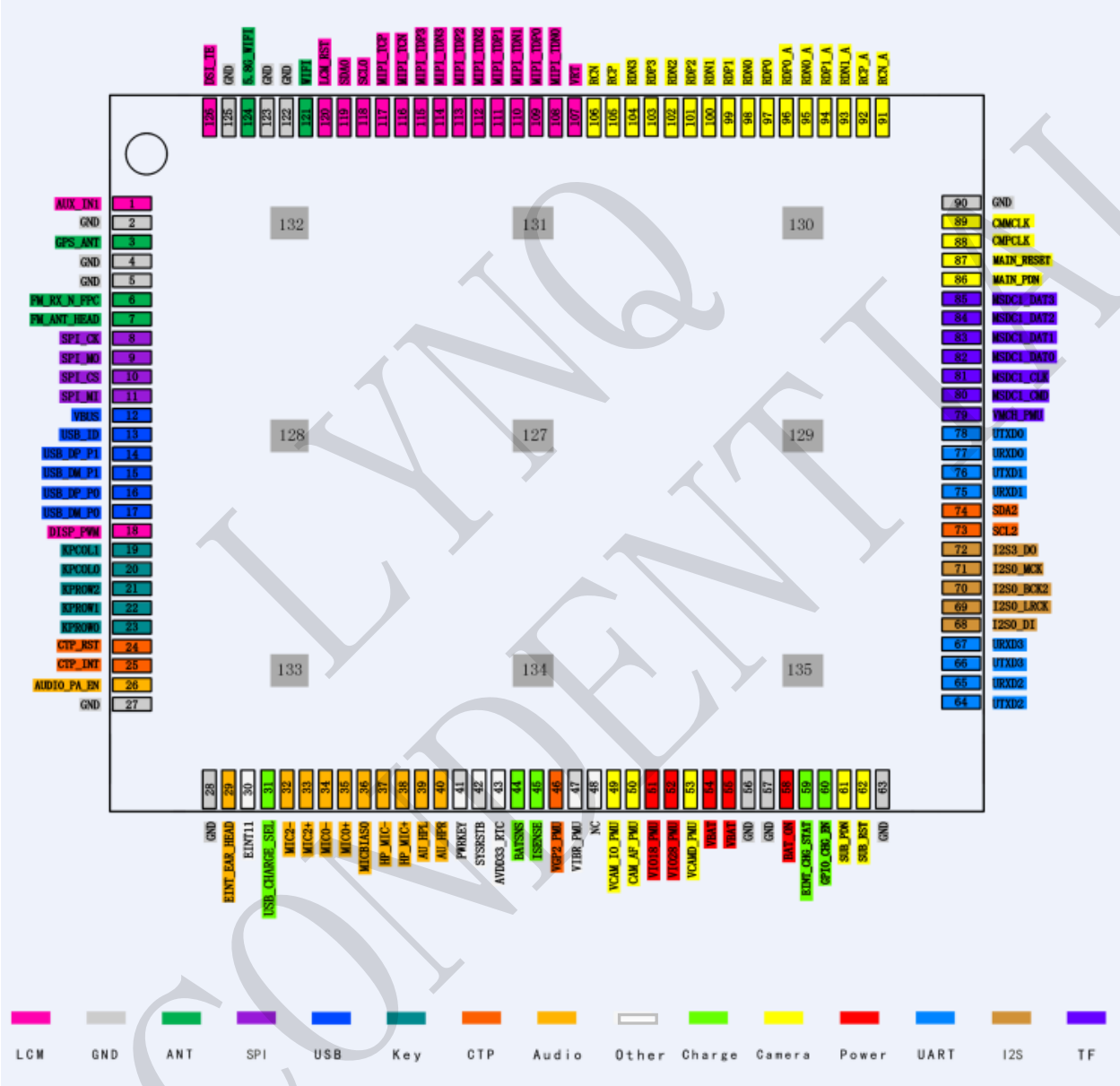


Figure 2-1 M1505 Top View

## 2.2 Pin Description

M1505 interface specific functions are as follows:

Table 2-1 Pin Description

| Pin NO. | Pin name | Type | Function Description | Power domain | State when not used(1) |
|---|---|---|---|---|---|
| 1 | AuxADC1 | I | ADC external input channel 1 | 0～1.45V | Open |
| 2 | GND | G | Ground | | Ground |
| 3 | GPS_ANT | I | GPS ANTENNA | | No Need |
| 4 | GND | G | Ground | | Ground |
| 5 | GND | G | Ground | | Ground |
| 6 | FM_RX_N_FPC | AI | FM differential RF input, negative terminal | | Open |
| 7 | FM_ANT_HEAD | AI | FM differential RF input, positive terminal | | Open |
| 8 | GPIO54 | I/O | General Purpose Input Output 54 | VIO18 | Open |
| 9 | GPIO56 | I/O | General Purpose Input Output 56 | VIO18 | Open |
| 10 | NFC_ENB | I/O | General Purpose Input Output 53 for NFC_ENB | VIO18 | Open |
| 11 | EINT_NFC | I/O | External interrupt 56 for EINT_NFC | VIO18 | Open |
| 12 | VBUS | P | USB 5V voltage input | 5V | Open |
| 13 | USB_ID | I | USB Identification | VIO18 | Open |
| 14 | USB_DP_P1 | DIO | USB port1 differential data line | | Open |
| 15 | USB_DM_P1 | DIO | | | Open |
| 16 | USB_DP_P0 | DIO | USB port0 differential data line | | Open |

| | | | | | |
|---|---|---|---|---|---|
| 17 | USB_DM_P0 | DIO | | | Open |
| 18 | DISP_PWM | I/O | Display PWM output | VIO18 | Open |
| 19 | KPCOL1 | DIO | Keypad column1 | VIO18 | Open |
| 20 | KPCOL0 | DIO | Keypad column0 | VIO18 | Open |
| 21 | KPROW2 | DIO | Keypad row2 | VIO18 | Open |
| 22 | KPROW1 | DIO | Keypad row1 | VIO18 | Open |
| 23 | KPROW0 | DIO | Keypad row0 | VIO18 | Open |
| 24 | TP_RST | I/O | General Purpose Input Output 29 for CTP reset | VIO18 | Open |
| 25 | TP_INT | I/O | External interrupt 9 for CTP | VIO18 | Open |
| 26 | AUDIO_PA_EN | I/O | General Purpose Input Output 50 for Audio PA enable | VIO18 | Open |
| 27 | GND | G | Ground | | Ground |
| 28 | GND | G | Ground | | Ground |
| 29 | EINT_EAR_HEAD | I/O | External interrupt 1 for headset | VIO18 | Open |
| 30 | SP232_EN | I/O | General Purpose Input Output 43 for SP232_EN | VIO18 | Open |
| 31 | CHARGE_SEL | I/O | General Purpose Input Output 26 for power source selection | VIO18 | Open |
| 32 | MIC2- | AI | Microphone Channel 2 | 0～3.08V | Open |
| 33 | MIC2+ | AI | | 0～3.08V | Open |
| 34 | MIC0- | AI | Microphone Channel 0 | 0～3.08V | Open |
| 35 | MIC0+ | AI | | 0～3.08V | Open |
| 36 | MICBIAS0 | P | Microphone Bias Voltage | 0～3.08V | Open |
| 37 | HP_MIC- | AI | Microphone Channel For Earphone | 0～3.08V | Open |
| 38 | HP_MIC+ | AI | | 0～3.08V | Open |

| | | | | | |
|---|---|---|---|---|---|
| 39 | AU_HPL | AO | Earphone channel output | -1.98～1.98V | Open |
| 40 | AU_HPR | AO | | | Open |
| 41 | PWRKEY | I | Powerkey button | 0～4.5V | Open |
| 42 | SYSRSTB | I | System reset signal | 1.8V | Open |
| 43 | RTC | P | RTC LDO output. Supply of RTC macro where backup battery can be added | 3.3V | Open |
| 44 | BATSNS | I | Negative terminal for battery's charging current sensing resistor | 2.5～4.5V | Connect to VBAT |
| 45 | ISENSE | I | Positive terminal for battery's charging current sensing resistor | 2.5～4.5V | Connect to VBAT |
| 46 | VGP2_CTP | P | VGP2 output voltage for TP | 1.2/1.3/1.5/1.8/2.0/2.5/2.8/3.0V | Open |
| 47 | VIBR_PMU | P | Vibrate output voltage | 1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3V | Open |
| 48 | NC | | NC | | |
| 49 | VCAM_IO_PMU | P | Camera IOVDD output voltage | 1.8V | Open |
| 50 | CAM_AF_PMU | P | VCAM AF output voltage | 1.2/1.3/1.5/1.8/2.0/2.8/3.0/3.3V | Open |
| 51 | VIO18_PMU | P | 1.8V output voltage | 1.8V | Open |
| 52 | VIO28_PMU | P | 2.8V output voltage | 2.8V | Open |
| 53 | VCAMD_PMU | P | Camera DVDD output voltage | 1.2/1.3/1.5/1.8V | Open |
| 54 | VBAT | P | Power Supply | 3.50~4.35V | Open |

| | | | | | |
|---|---|---|---|---|---|
| 55 | VBAT | | | | |
| 56 | GND | G | Ground | | Ground |
| 57 | GND | G | Ground | | Ground |
| 58 | BAT_ON | I | Battery NTC pin for battery and its temperature sensing | | Open |
| 59 | CHG_STAT | I/O | External interrupt 21 for Charge | VIO18 | Open |
| 60 | CHG_EN | I/O | General Purpose Input Output 49 for charge enable | VIO18 | Open |
| 61 | SUB_PDN | I/O | General Purpose Input Output 47 for sub camera powerdown | VIO18 | Open |
| 62 | SUB_RST | I/O | General Purpose Input Output 48 for sub camera reset | VIO18 | Open |
| 63 | GND | G | Ground | | Ground |
| 64 | UTXD2 | I/O | UART2_TX | VIO18 | Open |
| 65 | URXD2 | I/O | UART2_RX | VIO18 | Open |
| 66 | UTXD3 | I/O | UART3_TX | VIO18 | Open |
| 67 | URXD3 | I/O | UART3_RX | VIO18 | Open |
| 68 | GPIO72_CAMA | I/O | General Purpose Input Output 72 for camera AVDD enable | VIO18 | Open |
| 69 | FLASH_EN | I/O | General Purpose Input Output 73 for FLASH_EN | VIO18 | Open |
| 70 | NFC_RST | I/O | General Purpose Input Output 74 for NFC_RST | VIO18 | Open |
| 71 | NFC_IRQ | I/O | General Purpose Input Output 5 for NFC_IRQ | VIO18 | Open |
| 72 | GPIO52 | I/O | General Purpose Input Output 52 | VIO18 | Open |
| 73 | SCL2 | I/O | IIC2 clock | VIO18 | Open |

| | | | | | |
|---|---|---|---|---|---|
| 74 | SDA2 | I/O | IIC2 data | VIO18 | Open |
| 75 | URXD1 | I/O | UART1_RX | VIO18 | Open |
| 76 | UTXD1 | I/O | UART1_TX | VIO18 | Open |
| 77 | URXD0 | I/O | UART0_RX | VIO18 | Open |
| 78 | UTXD0 | I/O | UART0_TX | VIO18 | Open |
| 79 | VMCH_PMU | P | VMCH output voltage | 3.0/3.3V | Open |
| 80 | MSDC1_CMD | I/O | SD card command pin | DVDD28_MSDC1 | Open |
| 81 | MSDC1_CLK | I | SD card clock output | | Open |
| 82 | MSDC1_DAT0 | I/O | SD card data pin | | Open |
| 83 | MSDC1_DAT1 | I/O | | | Open |
| 84 | MSDC1_DAT2 | I/O | | | Open |
| 85 | MSDC1_DAT3 | I/O | | | Open |
| 86 | MAIN_PDN | I/O | General Purpose Input Output 117 for main camera powerdown | VIO18 | Open |
| 87 | MAIN_RST | I/O | General Purpose Input Output 118 for main camera reset | | Open |
| 88 | CMPCLK | I | Pixel clock from sensor | | Open |
| 89 | CMMCLK | I | Master clock to sensor | | Open |
| 90 | GND | G | Ground | | Ground |
| 91 | RCN_A | DI | CSI1 CLK lane N | VIO18 | Open |
| 92 | RCP_A | DI | CSI1 CLK lane P | | Open |
| 93 | RDN1_A | DI | CSI1 lane1 N | | Open |
| 94 | RDP1_A | DI | CSI1 lane1 P | | Open |
| 95 | RDN0_A | DI | CSI1 lane0 N | | Open |
| 96 | RDP0_A | DI | CSI1 lane0 P | | Open |
| 97 | RDP0 | DI | CSI0 lane0 P | | Open |



 

| | | | | | |
|---|---|---|---|---|---|
| 98 | RDN0 | DI | CSI0 lane0 N | | Open |
| 99 | RDP1 | DI | CSI0 lane1 P | | Open |
| 100 | RDN1 | DI | CSI0 lane1 N | | Open |
| 101 | RDP2 | DI | CSI0 lane2 P | | Open |
| 102 | RDN2 | DI | CSI0 lane2 N | | Open |
| 103 | RDP3 | DI | CSI0 lane3 P | | Open |
| 104 | RDN3 | DI | CSI0 lane3 N | | Open |
| 105 | RCP | DI | CSI0 CLK lane P | | Open |
| 106 | RCN | DI | CSI0 CLK lane N | | Open |
| 107 | VRT | / | Connect to 1.5K for MIPI display;<br>Connect to 24K for LVDS display | | Open |
| 108 | MIPI_TDN0 | DO | DSI0 lane0 N | VIO18 | Open |
| 109 | MIPI_TDP0 | DO | DSI0 lane0 P | | Open |
| 110 | MIPI_TDN1 | DO | DSI0 lane1 N | | Open |
| 111 | MIPI_TDP1 | DO | DSI0 lane1 P | | Open |
| 112 | MIPI_TDN2 | DO | DSI0 lane2 N | | Open |
| 113 | MIPI_TDP2 | DO | DSI0 lane2 P | | Open |
| 114 | MIPI_TDN3 | DO | DSI0 lane3 N | | Open |
| 115 | MIPI_TDP3 | DO | DSI0 lane3 P | | Open |
| 116 | MIPI_TCN | DO | DSI0 CLK lane N | | Open |
| 117 | MIPI_TCP | DO | DSI0 CLK lane P | | Open |
| 118 | SCL0 | I/O | IIC0 clock | VIO18 | Open |
| 119 | SDA0 | I/O | IIC0 data | VIO18 | Open |
| 120 | LCM_RST | I/O | Parallel display interface reset signal | VIO18 | Open |
| 121 | ANT_WIFI/BT | / | 2.4G/5G_WIFI/BT Antenna | | Open |

| | | | | | |
|---|---|---|---|---|---|
| 122 | GND | G | Ground | | Ground |
| 123 | GND | G | Ground | | Ground |
| 124 | NC | / | NC | | |
| 125 | GND | G | Ground | | Ground |
| 126 | DSI_TE | I/O | Parallel display interface tearing effect | VIO18 | Open |
| 127 | GND | G | Ground | | Ground |
| 128 | GND | G | Ground | | Ground |
| 129 | GND | G | Ground | | Ground |
| 130 | GND | G | Ground | | Ground |
| 131 | GND | G | Ground | | Ground |
| 132 | GND | G | Ground | | Ground |
| 133 | GND | G | Ground | | Ground |
| 134 | GND | G | Ground | | Ground |
| 135 | GND | G | Ground | | Ground |

(1) Suggested status when not in use.

Table 2-2 Pin Type Description

| | |
|---|---|
| P:POWER | AI:ANALOGY INPUT |
| G:GROUND | AO:ANALOGY OUTPUT |
| I:INPUT | DI:DIGITAL INPUT |
| O:OUTPUT | DO:DIGITAL OUTPUT |
| ANT:ANTENNA | DIO:DIGITAL INPUT OUTPUT |
| NC:NOT CONNECT | AIO:ANALOGY INPUT OUTPUT |

Notes：For more details, Please refer to the document“M1505_PIN_Formal _Application_Spec”.

## 2.3 Package Information

### 2.3.1 Dimensions

The M1505 mechanical dimensions are described as following figure (Top view, Side view ).

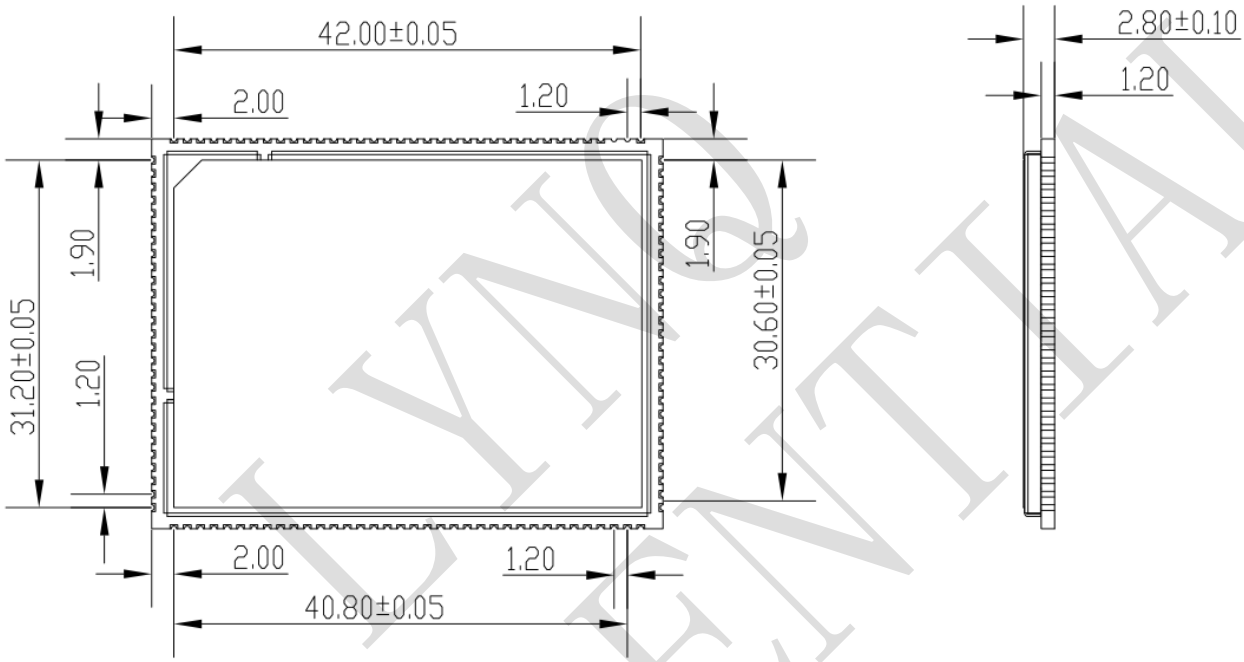


Figure 2-2 Mechanical Dimensions (Unit: mm)

### 2.3.2 Module size

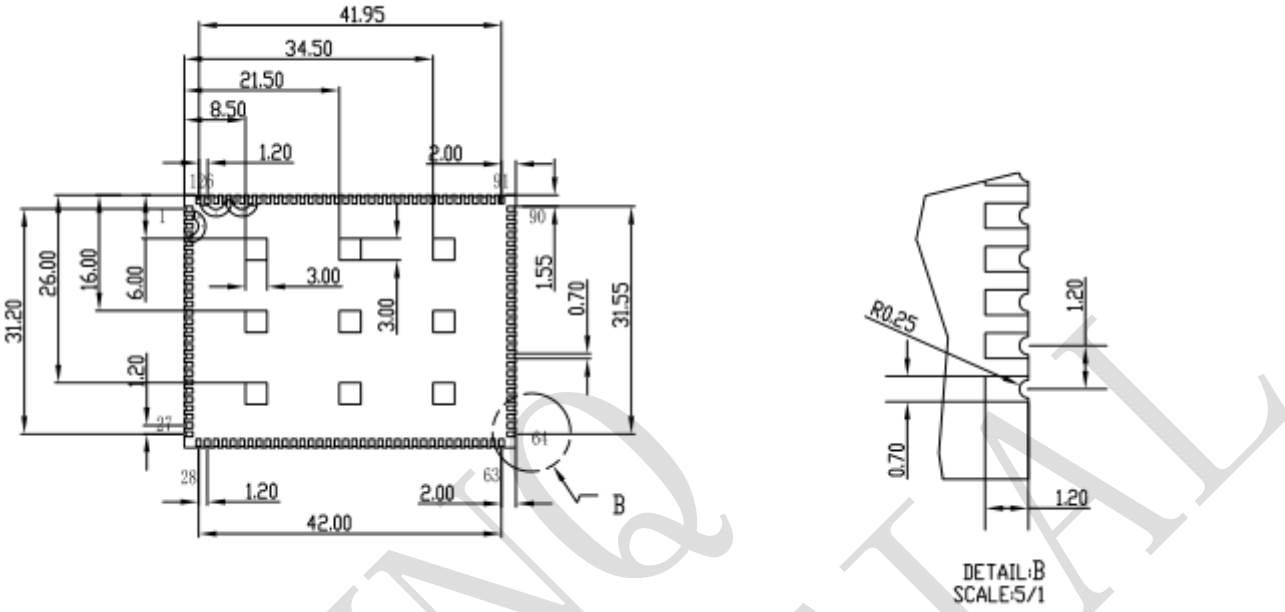


Figure 2-3 Module size

### 2.3.3 Recommend Pad

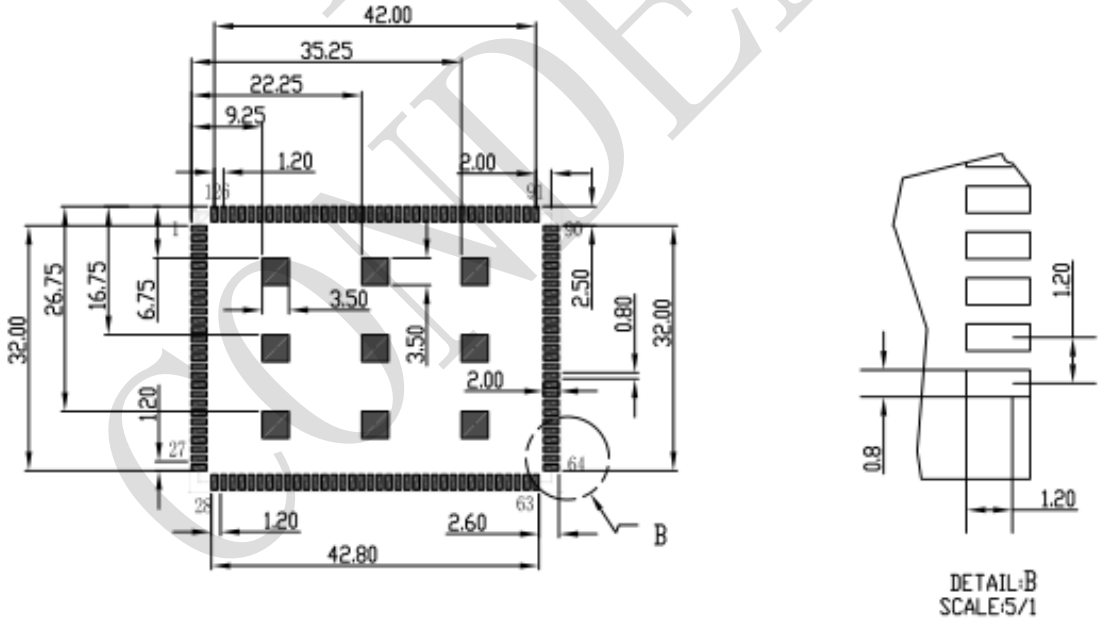


Figure 2-4 Recommended PCB layout package (Unit: mm)

# 3. Interface Circuit Reference Design

## 3.1 Power Section

### 3.1.1 Power Supply

VBAT is the main power supply module, and the input voltage range is 3.50V to 4.35V. The recommended voltage is 4.0V. Because the module transmit burst may cause voltage drops, the highest peak will reach 2.5A. A large capacitor is recommended to be used near VBAT pins, and the bigger of the capacitor's value is the better. In order to improve the continued flow of large current, it is recommended to use a low-impedance tantalum capacitor 470uF or larger. During layout, the capacitors are close to the VBAT pins.

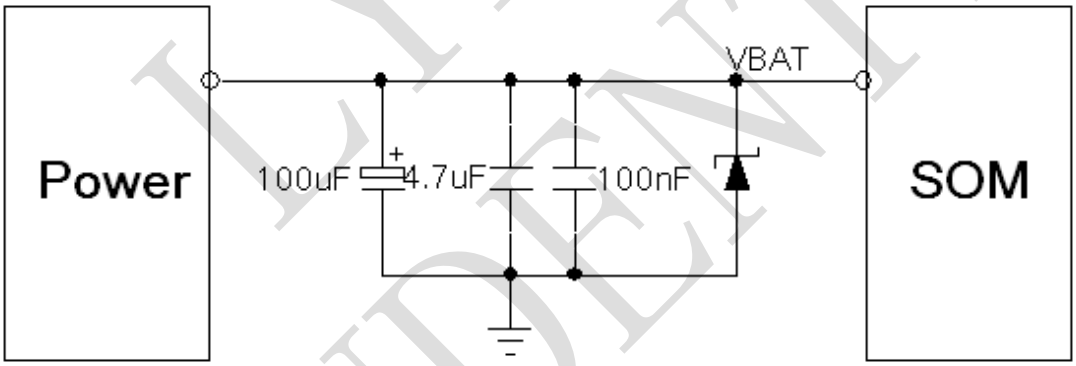


Figure 3-1 Reference circuit of the VBAT input

Notes: According to the environment, please select capacitor as large value as possible; and add 100pF, 33pF capacitors if requiring.

Add Zener close to our SOM. The Zener should be 5.1V/500mW, Ir<100uA @Vr=4.2V. Ta=25℃.

The Panel of VBAT should be close to SOM and the Layout of VBAT should be far away from the RF parts. The width of VBAT should be enough for 3A current. We suggest the width over 3mm and the power plane should be integral with enough GND via.

VBAT_M and BAT_ON are battery positive and sense pins.

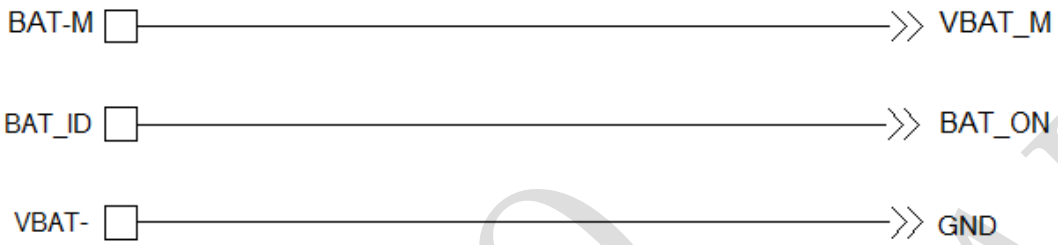


Figure 3-2 battery nets

### 3.1.2 Charge

BQ24196 is a USB charging IC, and lithium batteries can be charged. The maximum current for USB OTG can be provided for 500mA. ISENSE and BATSNS are battery current detection signals, with two 0Ω resistors closely connected to VBAT_M and VBAT pin.

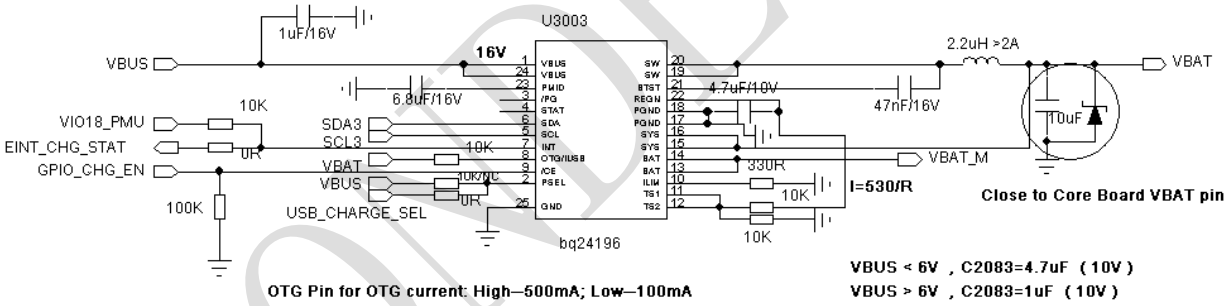


Figure 3-3 charging circuit

Notes: If customers don't use electricity quality detection function, BANSNS pin should be pulled up to VBAT. Or else, it will affect the download and power on.

### 3.1.3 Turn On/Off

Module 41-pin is the Power on/off key. Pulling down the PWRKEY at least 3-5 seconds and then releasing, the module will boot. There is internal pulled resistor.

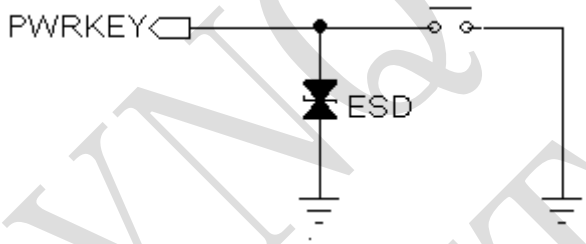


Figure 3-4 Turn on circuit

This net can also be used for hardware reset. When this pin has been pulled down over 11 seconds, the SOM will be reset.

### 3.1.4 Hardware Reset

Pin42 is hardware reset. When this pin is pulled down to GND, the SOM will shut down. It has internal pull-up to 1.8V.

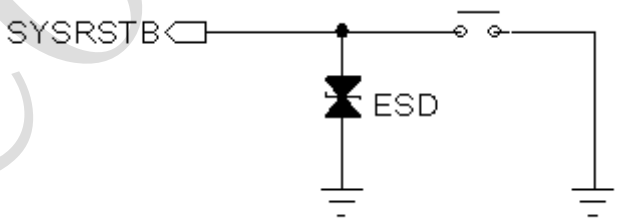


Figure 3-5 Reset key

Notes: Sysrstb can make the SOM power off, not reset the SOM.

Long press of Powerkey can reboot the SOM.

### 3.1.5 VRTC

The VRTC supply the power of the internal SOM RTC circuits. The SOM has a 22uF capacitive internally, which can support the time information during the battery change. However, the capacitive can only support about 10 seconds. If need longer time, a backup battery will be needed.

## 3.2 Audio Section

The SOM support several audio inputs and outputs, which can meet different audio demands. The audio must take the differential layout and must be protected by GND around it. The audio layout should be not parallel to other layout of power or high speed routes.

### 3.2.1 Audio input

Audio input includes main MIC, sub MIC and headset MIC.

(1) The SOM has MIC_BIAS signal. The circuits of Silicon MIC and common MIC are shown below. MIC signal needs differential traces.

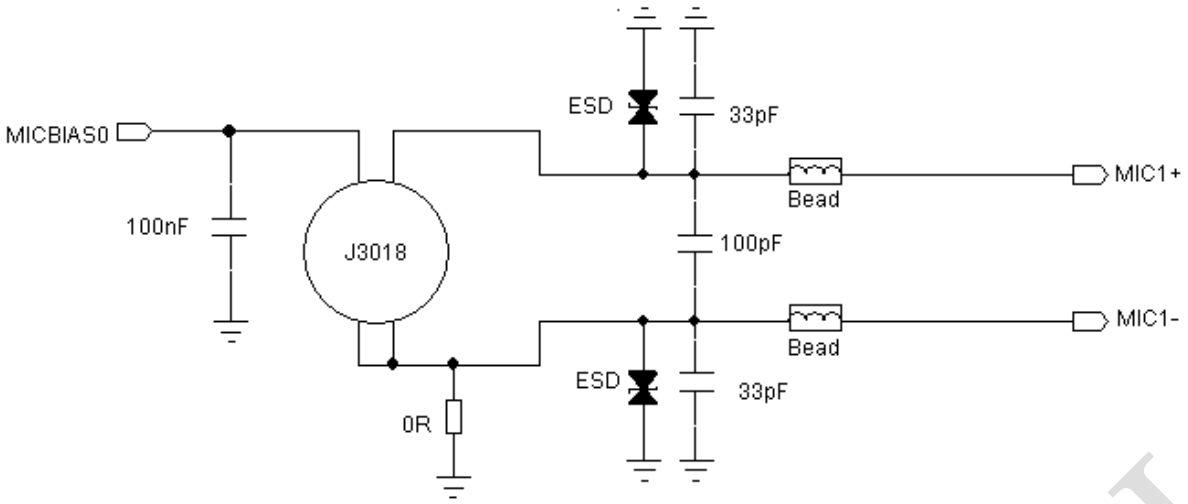


Figure 3-6 Main Silicon Mic circuit

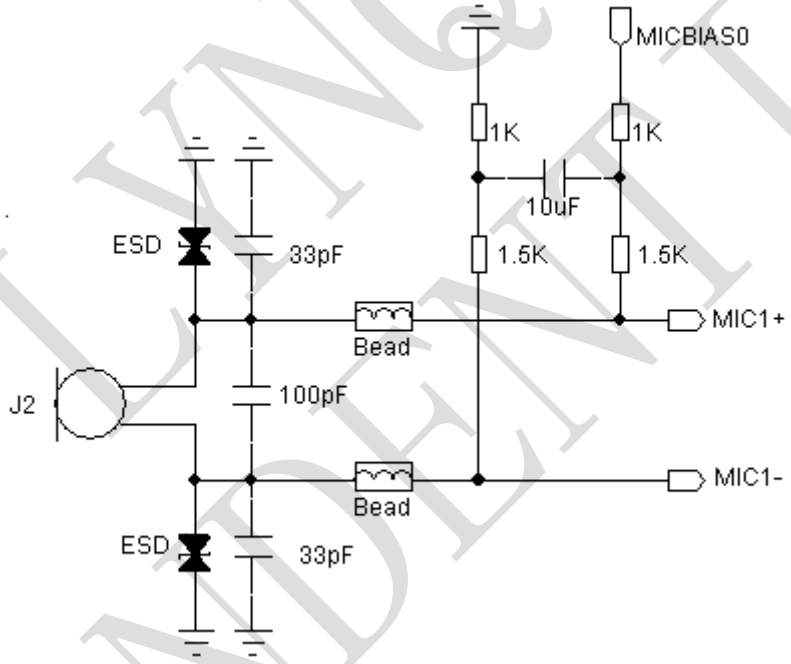


Figure 3-7 Main common MIC circuit

(2) The Sub circuit of the second MIC is same as the Main MIC circuit.

.The singles of sub MIC are MIC2+/MIC2-.

Notes: It doesn't work in hands-free calls, network call and recording state. It is stereo in recording state.

(3) Headphone reference circuit is shown below. Different components should be selected using American standard and European standard headset according to the actual needs. FM_RX_N_FPC and FM_ANT_HEAD signals are the radio antenna. When the earphone line is not use as FM antenna, FM_ANT_FPC can be used as internal antenna feed pad.

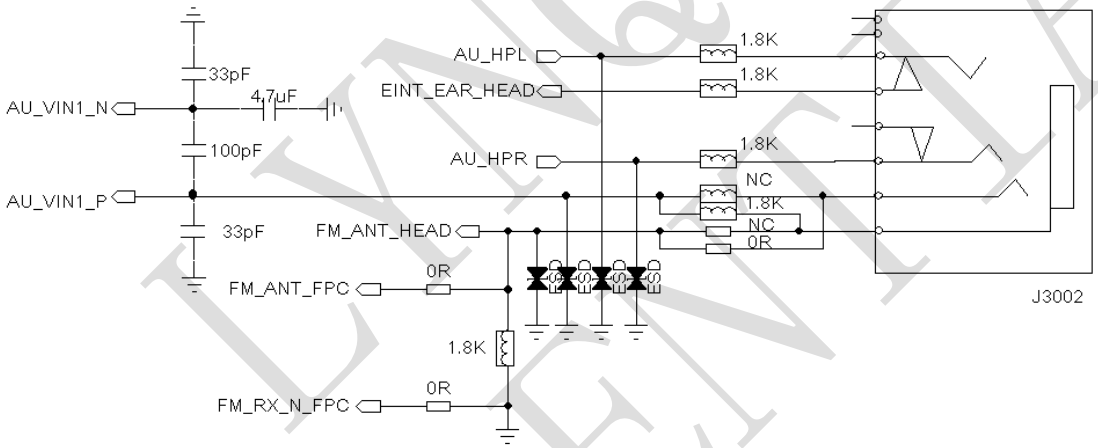


Figure 3-8 Headphone reference circuit

Notes: 1.8K Bead can't be changed to 1.8K resistor.

Bead can help to strong the FM _ANT performance.

### 3.2.2 Audio output

Audio output includes speaker and headset.

(1) SPEAKER circuits use the sixth generation of K class music amplifier AW8736 single-ended input mode, with a gain of 16 and a power of 0.8W, 1W or 1.2W. A speaker over 0.7W is recommended.

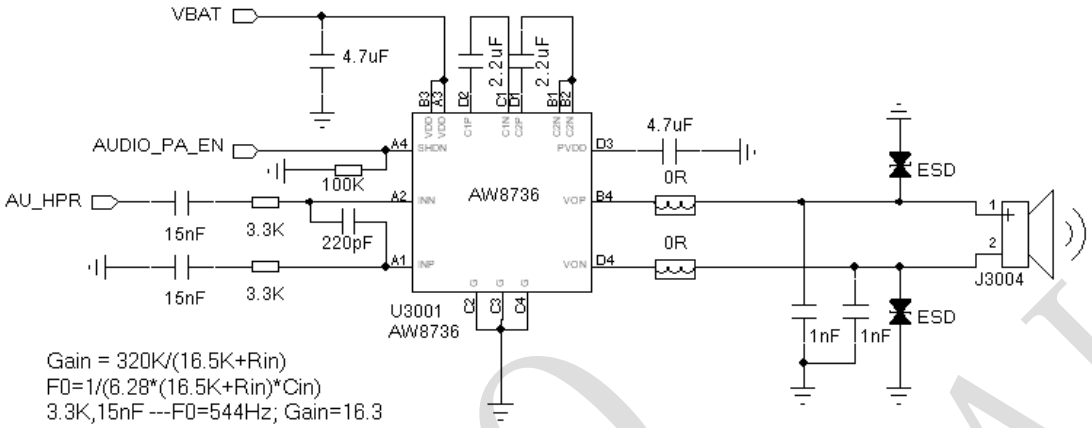


Figure 3-9 Speaker amplify circuit

(2) Headphone reference circuit refers as figure 3-8.

## 3.3 Interface Section

The main peripheral interfaces include antenna, TP, LCM, MIPI camera, USB, UART, TF card, SPI, Motor and keys.

### 3.3.1 Antenna interface

(1) WIFI/BT ANT

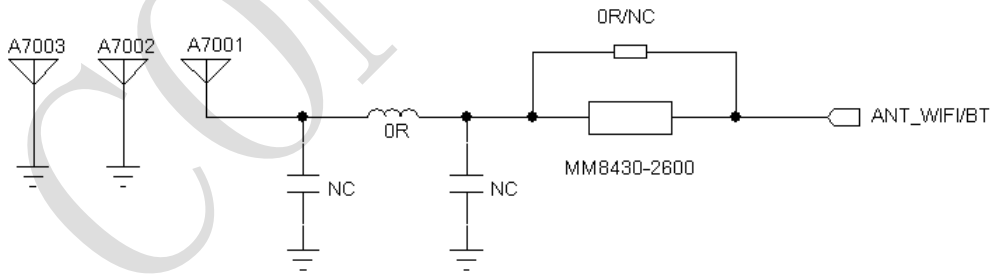


Figure 3-10 WIFI/BT ANT

(2) GPS ANT

ANT_GPS PI-type matche network connect to a coaxial connector or antenna contact, with the trance controled by 50-ohm impedance.

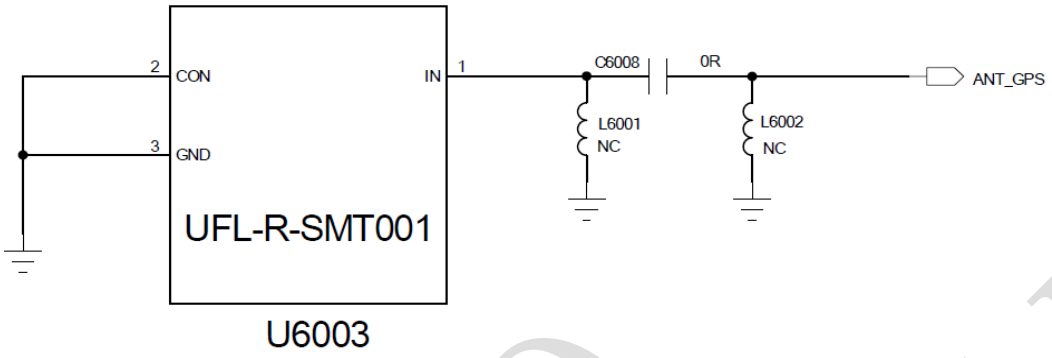


Figure 3-11 GPS ANT

(3) FM_ANT_FPC is built-in FM antenna PAD.


Figure 3-12 FM internal ANT

### 3.3.2 Display interface

The SOM supports MIPI_DSI and LVDS interface, which is up to FWXGA (1366*768) resolution.

(1) LCM interface and backlight driver

DISP_PWM0 is the duty cycle signal to adjust the brightness of the screen. The module output a high level greater than 1.4V can enable backlight.

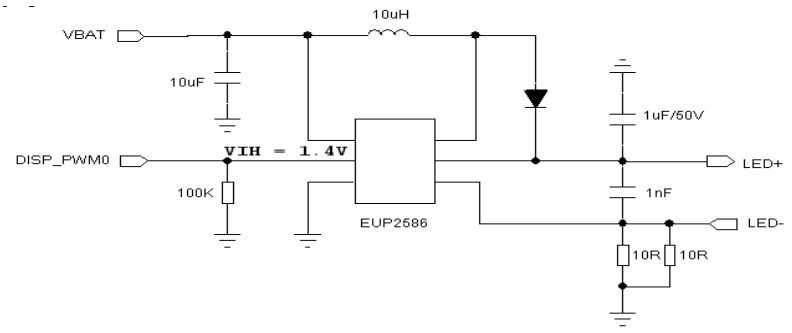


Figure 3-13 MIPI backlight driver circuit

MIPI screen is connected to the connector. The capacitor should be placed close to the power. Avoiding the current leakage, VIO18 and VIO28 are suggested to use external controllable LDO.

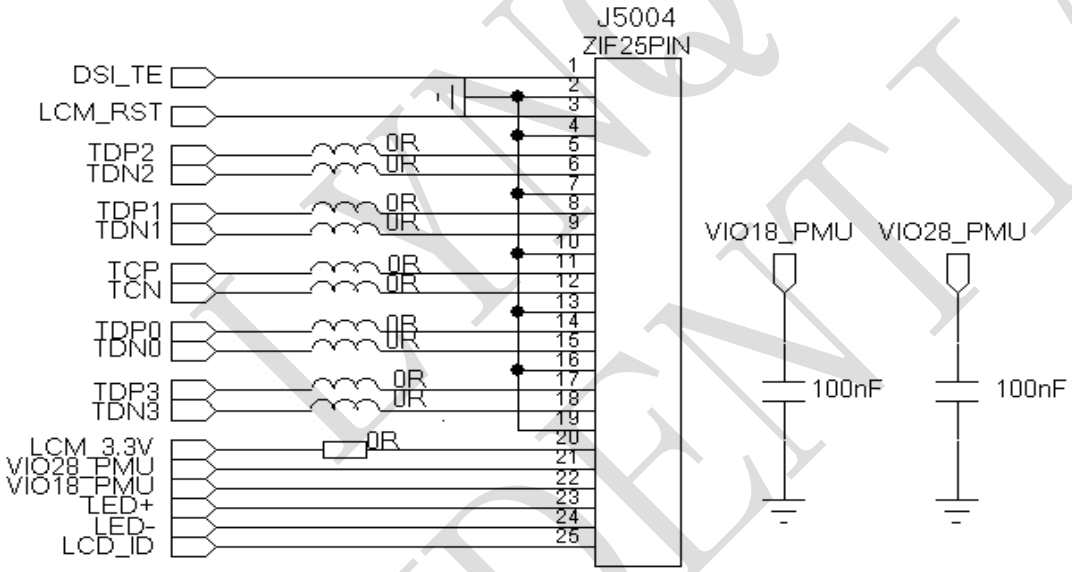


Figure 3-14 MIPI connector

Table 3-1 MIPI Panel corresponds to LVDS Panel interface

| Pin | MIPI Panel | LVDS Panel |
|---|---|---|
| 108 | MIPI_TDN0 | LVDS_TDN0 |
| 109 | MIPI_TDP0 | LVDS_TDP0 |
| 110 | MIPI_TDN1 | LVDS_TDN1 |

| | | |
|---|---|---|
| 111 | MIPI_TDP1 | LVDS_TDP1 |
| 112 | MIPI_TDN2 | LVDS_CLKN |
| 113 | MIPI_TDP2 | LVDS_CLKP |
| 114 | MIPI_TDN3 | LVDS_TDN3 |
| 115 | MIPI_TDP3 | LVDS_TDP3 |
| 116 | MIPI_TCN | LVDS_TDN2 |
| 117 | MIPI_TCP | LVDS_TDP2 |

Notes: Module supports MIPI and LVDS interfaces. When using MIPI interface, Pin107 (VRT) must have a 1.5K resistor in series. When using LVDS interface, Pin107 (VRT) must have a 24K resistor in series.

Some LVDS pins may be 3.3V so level shift would be needed in this condition.

(2) TP interface

Each TP signal is suggested to connect a test point for the measurement.

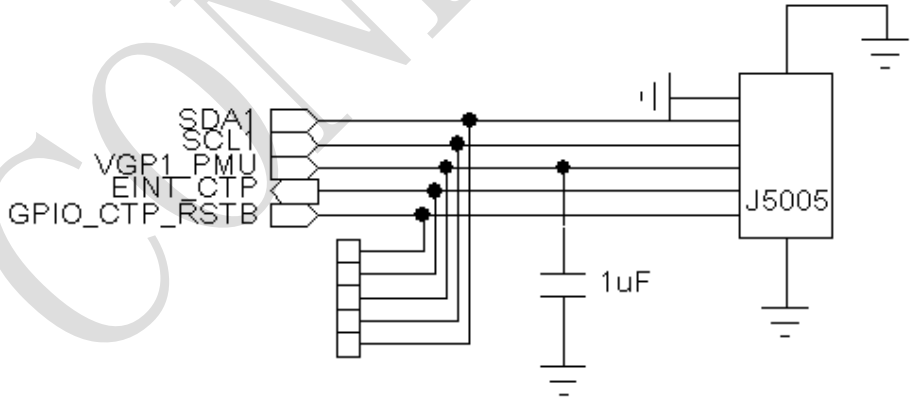


Figure 3-15 TP connector

### 3.3.3 Camera interface

Camera support MIPI interfaces and 8-bit parallel interfaces. Rear Camera supports 13MP@18fps and Front Camera supports 5MP@24fps. Please select the AVL of MTK to prepare your peripheral module.

(1) Main camera

It supports 4-Lane camera.

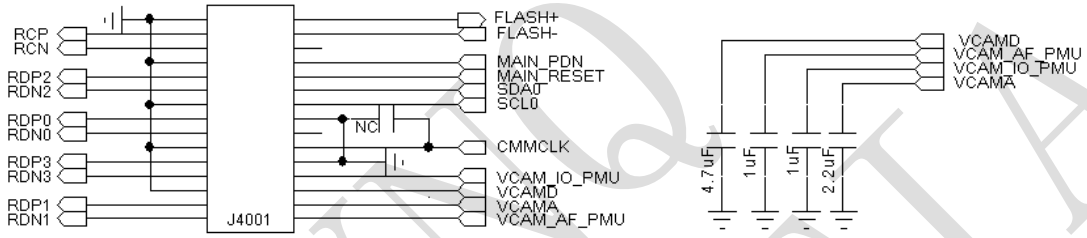


Figure 3-16 Rear Camera circuit

(2) Sub camera

Front camera only supports 2-Lane module.

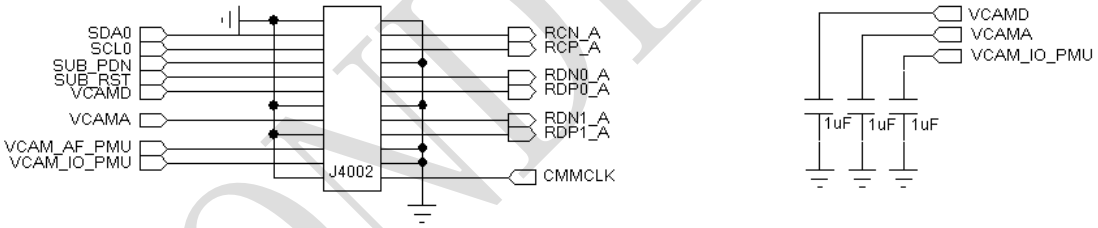


Figure 3-17 Front Camera circuit

Camera also supports 8-bit parallel interfaces, and can be extended to other functions. Show as follows.

Table 3-2 Camera parallel interfaces

| Pin | MIPI interface | 8-bit interface |
|---|---|---|
| 102 | RDN2 | I0*CMDAT8 |
| 101 | RDP2 | I0*CMDAT9 |
| 104 | RDN3 | I0*CMDAT4 |
| 103 | RDP3 | I0*CMDAT5 |
| 91 | RCN_A | I0*CMDAT6 |
| 92 | RCP_A | I0*CMDAT7 |
| 93 | RDN1_A | I0*CMDAT2 |
| 94 | RDP1_A | I0*CMDAT3 |
| 95 | RDN0_A | I0*CMHSYNC |
| 96 | RDP0_A | I0*CMVSYNC |

(3) Camera power

VCAMA 2.8V uses external LDO supply to get better camera effect. VCAMD_PMU is suggested to use external LDO also.

Table 3-3 Camera Power

| PIN name | Default voltage（V） | Vout（V） | Imax(mA) | Default on(Y/N) |
|---|---|---|---|---|
| VCAMA | 2.8 | 2.8 | 200 | N |
| VCAM_AF | 2.8 | 1.2/1.3/1.5/1.8/2.5/2.8/ 3.0/3.3 | 100 | N |
| VCAM_IO | 1.8 | 1.8 | 100 | N |

| | | | | |
|---|---|---|---|---|
| VCAMD | 1.5 | 1.2/1.3/1.5/1.8 | 150 | N |

Note：M1506 don’t support PIP function (picture in picture).

### 3.3.4 TF card interface

The SOM support 4-bit SD interfaces and SDIO2.0. Each TF signal should be protected by ESD components close to the connector. MSDC1_CLK signal should be protected by GND.

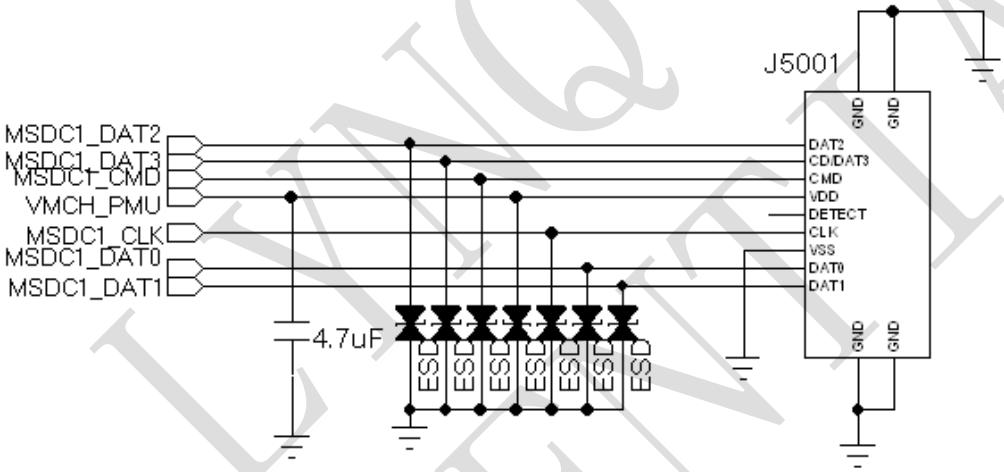


Figure 3-18 TF card circuit

Notes: The capacity value of ESD should be under 10pF. However, as NFC function, the value of ESD should be under 0.5pF.

### 3.3.5 USB interface

The SOM can download and transfer the data through USB interface. The circuit is as follow.

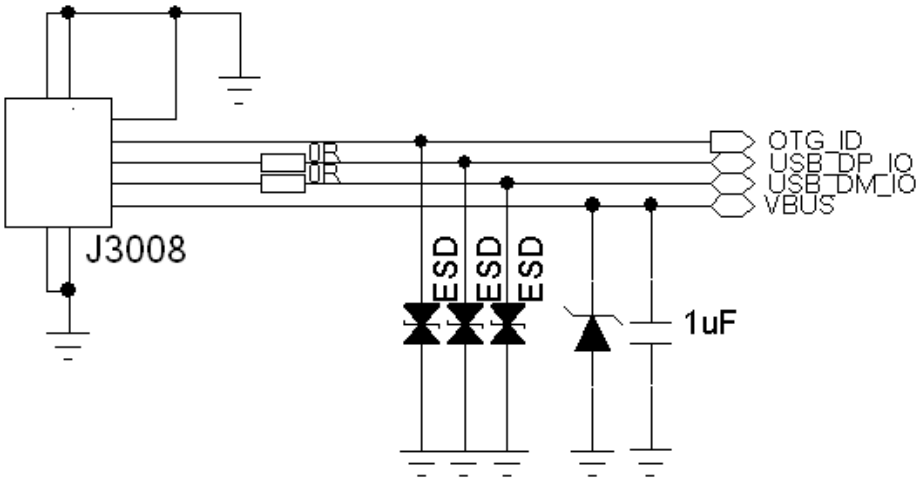


Figure 3-19 USB circuit

Table 3-4 USB Interface

| Pin Number | Pin Name | Description |
|---|---|---|
| 14 | USB_DP_P1 | USB port differential data line 1 |
| 15 | USB_DM_P1 | |
| 16 | USB_DP_P0 | USB port differential data line 0 |
| 17 | USB_DM_P0 | |

Notes：Select suitable voltage of ESD components alone VBUS, value of DP/DM ESD should be under 3pF.

USB routes should be differential and controlled with 90ohm resistor. It also should be protected around by GND and not be crossed with other routes.

Under the condition of supporting the USB OTG, a DCDC 5V Voltage output is demanded from the board. The Demo uses the BQ24196 to supply the 5V.

### 3.3.6 UART interface

Module provides 4 UART serial ports. Serial port 0 is for the system debugging. Because the module's serial port is 1.8V level, it should pay attention to match the IO level.

Notes: The voltage of UART is 1.8V so a level shift is needed for the UART using.

Similarly another level conversion connects to the DB9 connector through the 232 level shift IC.

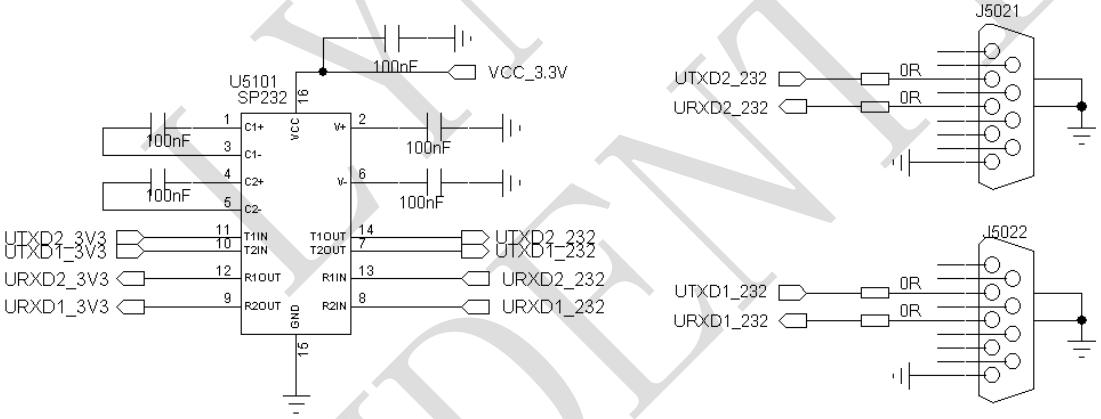


Figure 3-20 UART communication circuit

### 3.3.7 IIC interface

The Module can support 2 groups of IIC interfaces which are pulled up internally. IIC0 and IIC2 are pulled by VIO18.

Different IIC is suggested to use in different functions, seeing as follow table. Please note the address alone each IIC can't be the same.

Table 3-3 IIC Function selection

| | | |
|---|---|---|
| IIC0 | Rear Camera w AF<br>Front Camera w/o AF<br>TP | Open drain type |
| IIC2 | Mems sensors<br>NFC<br>Charger | Open drain type |

### 3.3.8 SPI interface

The module supports one SPI interface and is master device in default.

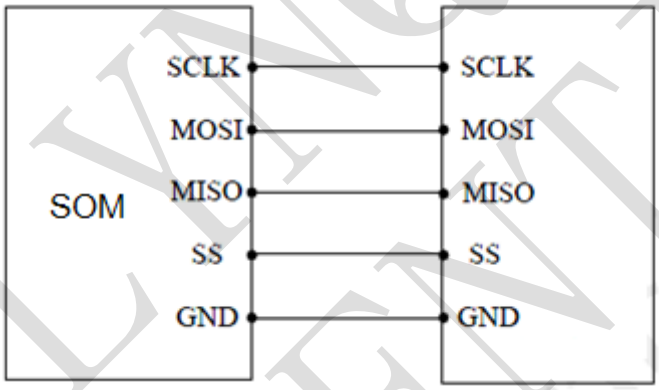


Figure 3-21 SPI connecting

Notes: SPI and IIC interfaces are 1.8V. If required, please use level shift.

### 3.3.9 Motor interface

The motor circuit is pretty simply only with a voltage supply.

If the motor is close to ANT, please add 33pF capacitive avoiding the motor's effect to the antenna.

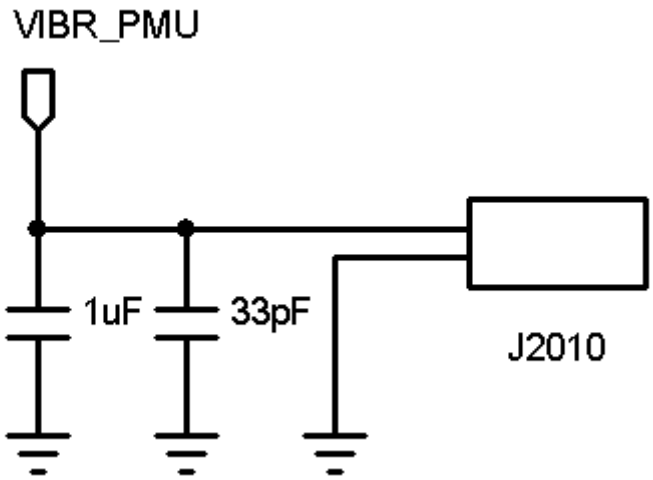


Figure 3-22 Motor circuit

### 3.3.10 Key interface

The module supports 2X3 X 2 keys.

KCOL0~1 and KROW0~2 can also be extended double keys. The figure is as follow, and the resistor is 20KR.

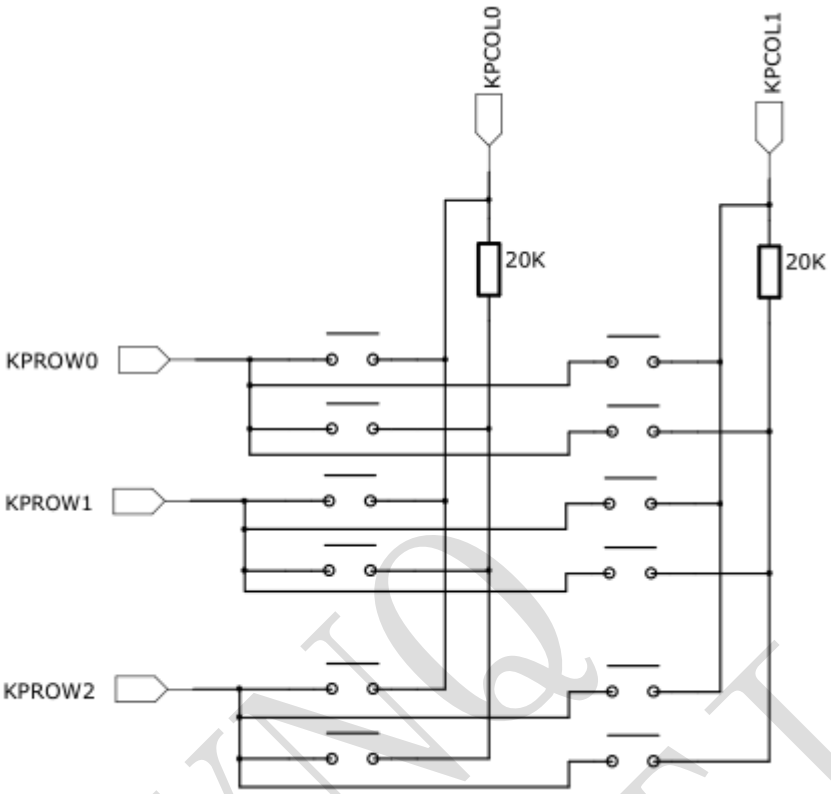


Figure 3-23 Key Extent

Notes: Suggest our customers to reserve test point of KCOL0 or use KCOL0 as an external key. When our customers have downloaded other software, KCOL0 connected to GND can help to download new software. However, it is scare to meet that.

### 3.3.11 ADC interface

The module supports two ADC ways. One detects the battery temperament through pin58 BAT_ON, and another detects the photo resistance and LCM ID through Pin1 AuxADC1.

The Max voltage of ADC is 1.45V with 12-bit accuracy.

Table 3-4 ADC value

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input range | 0.05 | | 1.45 | V |

Notes: The Max voltage of ADC is 1.45V with 12-bit.

# 4. Electrical Characteristics

## 4.1 Electrical Characteristic

Table 4-1 Electrical Characteristic

| Power | Min. | Nom. | Max | Unit |
|---|---|---|---|---|
| VBAT | 3.5 | 4.0 | 4.35 | V |
| Peak current | -0.3 | - | 2.5 | A |

Notes: The over-low voltage can't power on the module; Over-high voltage may be danger to damage the module.

Using the DCDC supply, please ensure the capacity of DCDC over 2.5A. We don't suggest the LDO as the power supplier.

## 4.2 Temperature

Table 4-2 Temperature Characteristic

| State | Min. | Nom. | Max | Unit |
|---|---|---|---|---|
| Working | -30 | 25 | 75 | ℃ |
| Storage | -40 | 25 | 85 | ℃ |

Notes: When the temperature is over the range, may cause power down or restart problem.

## 4.3 Maximum parameter

Table 4-3 Absolute maximum ratings for power supply

| Symbol or pin name | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| VIO18 | Power input for IO, MIPI CSI&DSI | 1.62 | 1.98 | V |
| DVDD28_MSDC1 | Digital power input for MSDC1 | 1.8 | 3.3 | V |

Notes: Stressing the device beyond the absolute maximum ratings may cause permanent damage.

## 4.4 Recommended Operating Conditions

Table 4-4 Recommended operating conditions for power supply

| Symbol or pin name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VIO18 | Power input for IO, MIPI CSI&DSI | 1.62 | 1.8 | 1.98 | V |
| DVDD28_MSDC1 | Digital power input for MSDC1 | 1.7 | 1.8 | 1.95 | V |
| | | 2.7 | 3.3 | 3.6 | |

Notes: All the GPIOs of SOM is 1.8V.

## 4.5 Power-on Sequence

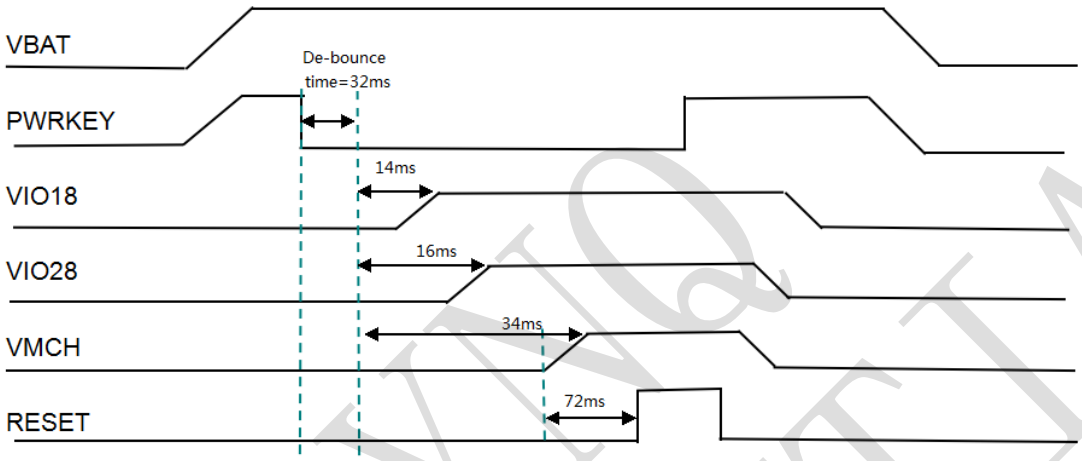


Figure 4-1 The power-on/off sequence by pressing PWRKEY

## 4.6 Digital IO characteristic

Table 4-5 Digital IO Voltage

| Parameter | Description | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|
| VIH | High level input voltage | 1.62 | 1.8 | 1.98 | V |
| VIL | Low level input voltage | 0 | - | 0.3 | V |
| VOH | High level output voltage | 1.62 | 1.8 | 1.98 | V |
| VOL | Low level output voltage | 0 | - | 0.3 | V |

Notes: Suit to all GPIO, IIC, UART, SPI interfaces.

## 4.7 Power consumption

Table 4-6 Power Consumption

| Parameter | Conditions | Min. | Average | Max. | Unit |
|---|---|---|---|---|---|
| Standby current | Power off mode | - | 0.075 | | mA |
| | Flight mode Suspend state | - | 2.6 | | mA |
| | Flight mode on WIFI | - | 3.2 | | mA |
| | Flight mode on BT | - | 3.6 | | mA |
| | Flight mode on GPS | - | 2.6 | | mA |
| Peak current | Max power mode burst current | | - | 2.5 | A |

## 4.8 ESD protection

The module contains highly sensitive electronic circuitry and is Electrostatic Sensitive Device. So, more attention should be paid to the procedure of handling and packaging. The ESD test results are shown in the following table.

Table 4-7 ESD Performance

| PIN | Contact discharge | Air discharge |
|---|---|---|
| VBAT | ±4KV | ±8KV |

| | | |
|---|---|---|
| GND | ±4KV | ±8KV |
| RF_ANT | ±4KV | ±8KV |

ESD performance（Temperature:25℃,humidity:45%）.

The methods of strengthen the ESD performances are as follows:

1. The metal of LCM should be connected well to GND; The FPC of LCM should be covered by shaded films which must be connected well to GND.
2. Reserve ESD on the CTP circuits.
3. If a converted board is added, it should have enough GND pins and be equally distributed. And the Layout of GND should be enough wide.
4. Floating small board (like key or led board ) should be connected well to GND.
5. Keys should be increased ESD components. The routes of power key and reset key should be far away from the sides of the board.
6. The audio circuits should be added ESD components close to audio peripherals. If using TVS components, TVS should be bi-directions.
7. USB, UART and other plug-in cable should be increased ESD components. Other control signals pulled out from the machine should also be added the ESD components.
8. SIM and TF card should be added ESD protect.
9. External Antenna should be added ESD protect.

Notes: For ESD protect, please add ESD methods according to upper ways.

High speed circuits like USB, TF and SIM card should be added ESD with low capacity value. Please note the voltage of ESD used in power like VBUS.

ESD components have Varistor and TVS. For better performance, please use TVS.

# 5. RF Features

## 5.1 RF Features Introduction

### 5.1.1 WLAN

The main WLAN features of the product are as follows：

a) Support 802.11a/b/g/n, 2.4G/5GHz dual frequency WIFI;

b) Support WIFI, Bluetooth single antenna design;

c) Support 2.4GHz max 15dBm and 5GHz max 12dBm transmit power;

d) Support for power control by internal detection;

e) Support self-calibration.

### 5.1.2 Bluetooth

a) Support Bluetooth V2.1+EDR;

b) Support Bluetooth V3.0;

c) Support Bluetooth V4.0+LE;

d) Support CLASS 1 Bluetooth transmission power rank.

### 5.1.3 FM

a) Support FM 65-108MHz Band，50KHz stepping;

b) Support RDS/RBDS;

c) Support FM 2-wire bus;

d) Support fast search.

### 5.1.4 GPS

a) Support GPS;

b) Support active / passive antenna.

## 5.2 RF Circuit Design

The connecting part of the radio frequency antenna of the product supports the PAD welding disc form, as shown in Figure 5-1.

The antenna interface between the core plate antenna and the customer main board is welded by the welding plate. Then it is connected through a microstrip line or a strip line. Which is designed by the characteristic impedance of 50 ohm, the length of the line is less than 10mm, and the L - type matching circuit is reserved.

This product antenna peripheral circuit design, the proposed RF circuit Layout program: RF line trances top layer, a reference to the second layer. Users need to pay attention to the design of the PCB line: to ensure the RF has full reference GND layer.

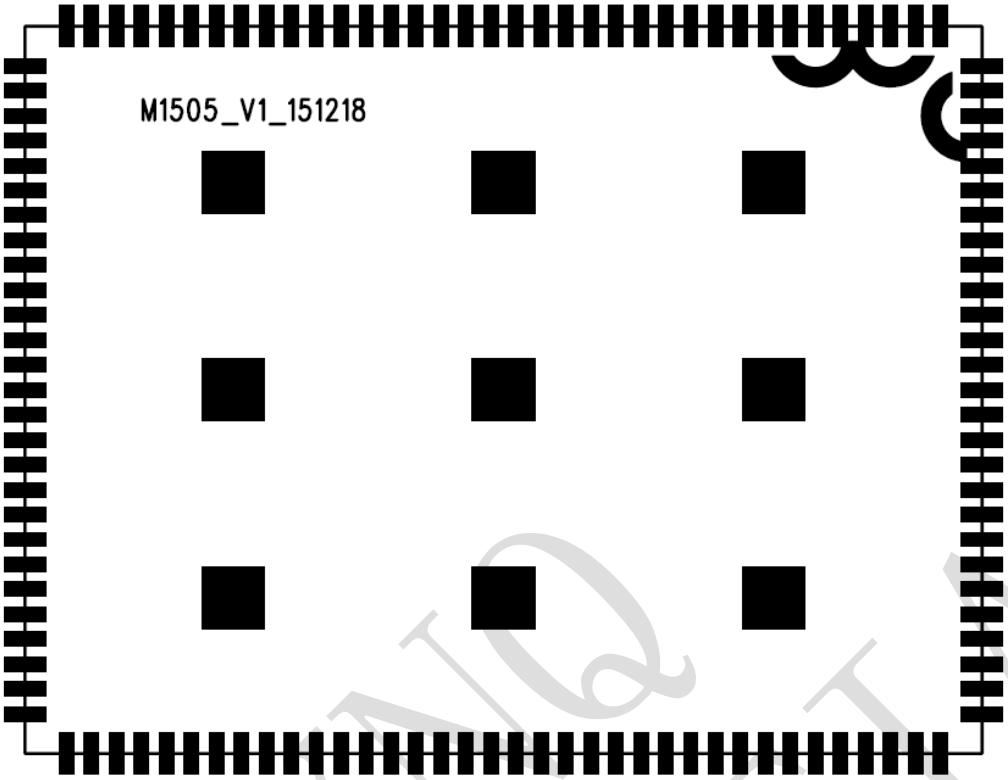


Figure 5-1 antenna RF connector interface

If the WLAN and GPS antenna path is longer (more than 10mm), it is recommended to use the RF connector (Figure 5-2), with the cable (Figure 5-3). The corresponding RF interface cable is suggested to use W.FL-LP-04N of HRS company. By this way, the antenna RF connector can be directly clamped on the RF test seat, which can realize long distance switching between RF antenna port and the interface of module.

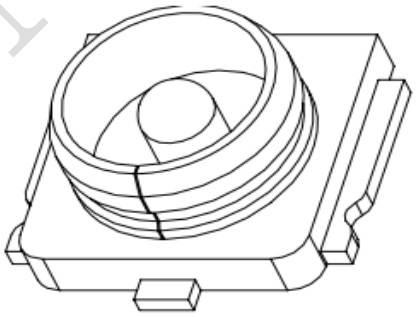

Figure 5-2 RF connector

Figure 5-3 RF cable

## 5.3 Initial attention to antenna design

a) Pre project evaluation

The choice of antenna position should far away from the switch power supply, data line, chip to place. At the same time, it should be avoided that the hand can be placed in the position of the antenna, which prevents the human body to produce attenuation; moreover, it must be considered to reduce the radiation and the structure of the realization. Therefore, in the design of the initial need for structure, ID, circuit, antenna engineers together to evaluate the layout..

b) Antenna occupancy space recommendations

WLAN_ANT area > 20mm (length) * 10mm (width) * 3mm (thick). GPS Antenna select 25*25 or 35*35 ceramics antenna.

c) SOM Layout

The experimental results show that the module is placed in the disturbed area, resulting in poor performance. Design is best when the module and the main board PCB separation, rather than on the main board. If you cannot make the separation, the module should be as far as possible from the chip and memory, power interface, data cable interface, camera FPC, screen FPC, connector FPC, and other possible EMI modules and devices. If close to the interference, It needs to set aside EMI

devices in the interface, and FPC needs double brush shield connected to the ground.

d) Antenna RF connector

Antenna RF cable traces must be as short as possible, 10mm can take the line, more than 10mm need to refer to the use of 5-2 connector. Taking the transmission loss into account, we propose the use of a thick point of RF line. At the same time, it should be far away from the chip and memory, power supply interface, data interface and so on, which may produce EMI module and device. Can't traces at an acute angle, cannot be squeezed, wear. Traces of RF should refer to the main ground of board.

e) Antenna matching circuit

If the RF antenna port of module and the antenna interface need switch, The microstrip or stripline between the test seat and the antenna interface must designed impedance 50 ohm and reserved L type matching circuit.

f) Selection of coaxial cable and RF connector

Antenna RF connection line usually use GBE in Taiwan (TW) and Shenyu, you can also consider Japan Somitomo, Shin DIN.4G antenna RF cable is generally used 1.37mm wire diameter. Antenna RF connectors generally used in Japan IPX, but also the use of HRS, but the price is a little high. The price is a little high.

# 6. Storage and Production

## 6.1 Storage

The rank of moisture proof of the SOM is level 3. There is an obvious sign on the table of the internal and the external packaging.

In the vacuum sealed bag, the SOM can be stored for 120 days when the temperature is 18°C～28°C and the humidity is 40~65%.

## 6.2 Production

The SOM is a humidity sensitive device. If the device needs reflow soldering, disassembly and maintenance, we must strictly comply with the requirements of humidity sensitive device. If module is damp, a reflow soldering or using a hot-air gun maintenance will lead to internal damage, because the water vapor has the rapid expansion of the burst, causing physical injury to the device, like PCB foaming and BGA component fail. So customers should refer to the following recommendations.

### 6.2.1 Module confirmation and moisture

The SOM in the production and packaging process should be strictly accordance with the humidity sensitive device operation. The factory packaging is vacuum bag, desiccant, and humidity indicator card. Please pay attention to the moisture control before SMT and the confirmation of the following aspects.

**Product packaging confirmation**

In order to ensure quality, smart module uses vacuum packaging and shipment, to avoid the question of SMT and function for the moisture in the air. Therefore, the requirements to confirm for the packaging of products before the SMT are necessary, ensuring the packaging not damaged, vacuum packing not leaks. If there is any breakage and leakage, the Module should be baked, to avoid PCB

foaming, BGA chip.

### Production cycle confirmation

The customer needs to confirm the production cycle of the product when receiving the product. If it exceed the storage period or the product has been affected with damp, the product must be baked. If the storage time not extended, and after opening the packaging, humidity indicator card is at 10% without discoloration, it indicate good packaging and can be normally used.

### Humidity indicator card confirmation

If the module has according to the moisture level 3 processing, and internal packaging have been placed humidity indicator cards, customers should confirm the humidity indicator card before SMT. If the humidity indicator card has changed more than 10%, it need to carry on the material baking.

### Baking condition confirmation

The moisture proof level of the smart module is level 3. And the baking conditions are as follows:

Table 6-1 Baking conditions

| **Baking conditions** | **90°/ 5%RH** | **60°/ 5%RH（Recommended）** | **40°/ 5%RH** |
|---|---|---|---|
| Baking time | 48 hours | 72 hours | 30days |
| Description | not use the original tray | not use the original tray | Can use the original tray |

Customers can also choose baking conditions according to their own conditions. But please refer to Level 3 and device thickness 1.4 ~ 2.0mm standard.

Notes: The original anti-ESD tray temperature does not exceed 50℃. Otherwise the tray will be deformed.

The anti-ESD tray of the original packaging is only used for packaging, and can't be used as a SMT tray.

### Factory life confirmation

Module SMT with good humidity control should be completed in 48 hours after opening the package. The unused Module should be vacuum packaging, and placed in a drying box. If exposure to air for more than 48 hours, the module need to be baked. Due to the larger size of the module, damp needs to bake for a long time, and the price is high, so please try to run out after opening the package.

### Customer product maintenance

If maintenance module after SMT, it is easy for damp module to damage when removing, so the module disassembly and other related maintenance operations should complete within 48 hours after SMT, or need to bake and then maintenance the module.

Because the module return from the field work can't ensure the dry state, it must be baked in accordance with the conditions of baking, then for disassembly and maintenance. If it has been exposed to the humid environment for a long time, please properly extend the baking time, such as 125 degrees /36 hours.

### 6.2.2 SMT reflow attentions

The module has the BGA chips, chip resistances and capacitances internally, which will melt at high temperature. If module melt completely encountered a large shock, such as excessive vibration of reflux conveyor belt or hit the board, internal components will easily shift or be false welding. So, using intelligent modules over the furnace need to pay attention to:

- Modules can't be vibrate larger, namely customer requirements as far as possible in orbit (chain)

furnace, furnace, avoid on the barbed wire furnace, in order to ensure smooth furnace.

- The highest temperature can't too high. In the condition that meet the welding quality of customer motherboard and module, the lower furnace temperature and the shorter maximum temperature time, the better.

Some customer's temperature curve in the line is not suitable, high temperature is too high, and customer motherboard melt good, but non-performing rate is on the high side. Through the analysis of the causes, it found that melt again of BGA components lead device offset and short circuit. After adjusting the temperature curve, it can ensure that the customer's motherboard the welding quality, and also improve the pass through rate. Non-performing rate is controlled below the 2/10000.

### 6.2.3 SMT stencil design and the problem of less tin soldering

Part of customers found false welding or circuit short when reflowing. The main reason is module tin less, PCB distortion or tins too large. Suggestions are as follows:

- Suggest use ladder stencil 0.10-0.18mm, which means the region of module is proposed to 0.18mm stencil thickness. Please adjust validation according to the measured thickness of solder paste, the actual company conditions and experience value. The products need to strictly test.

- Stencil: Reference module package and the user can adjust according to their company experience. Outside of the module, the stencil extends to 0.3mm outside. The GND pads use the net stencil.

In the production process, if you cannot judge the opening or process conditions, you can also contact our sales or after-sales service. We will give specific recommendations according to the actual situation.

### 6.2.4 SMT attentions

If customer motherboard is thin and slender with a furnace deformation, warping risks, you will be

suggested to create "a furnace vehicle" to ensure the welding quality. Other production proposals are as follows:

- The solder pastes use brands like Alfa.
- The module must use the SMT machine mount (important), and do not recommend manually placed or manual welding.
- Please strictly control the pressure and speed in SMT (very important).
- We must use the reflow oven more than 8 temperature zones, and strictly control the furnace temperature curve.

Recommended temperature:

B. constant temperature zone: temperature 160-190°C, time: 60s-100s

E. recirculation zone: PEAK temperature 235-245°C, time over 220°C: 30s-60s

Notes: Customer's board deformation must be controlled within 0.15mm. By reducing the number of imposition or increasing patch clamp to reduce the deformation.

SOM thickness of the stencil is recommended to be thickened to 0.18mm, and the rest position can be maintained by 0.1mm.