Approval Sheet

Customer	
Product Number	**M0UB-56PA1C03-J**
Module speed	**PC-133**
Pin	**168 Pin**
CAS Latency	**CL-3**
SDRAM Operating Temp.	**0 °C ~ 70 °C**
Date	**9th April 2014**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr. Technical Manager: John Hsieh**

Rev 1.0

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	CL=3			
PC-133	**B**	100	-	133	20	20	65

- Single Pulsed RAS- interface
- Fully Synchronous to positive CLK edge
- 4 banks controlled by BA0 & BA1
- Multiple Burst Read with single write option
- Automatic and controlled precharge command
- Auto refresh (CBR) and Self-Refresh
- JEDEC Standard 168-pin Memory Module
- Intend for 133 MHz applications
- Inputs and Outputs are LVTTL compatible
- VDD=VDDQ= 3.3 Volt ± 0.3
- Serial Presence Detect with EEPROM
- SDRAM Operation Temperature *(Note 1)*
  - –0°C ≤ T_A ≤ +70°C
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency:3
  - Burst Length: 1, 2, 4 or 8
- RoHS Compliant *(Section 13)*

Note:*1. The refresh rate is required to double when T_A Exceeds70°C.*

2. SDRAM Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +55	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	

1. The refresh rate is required to double when T_C exceeds 85°C.

3. Ordering Information

SDR-133 UDIMM						
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M0UB-56PA1C03-J	256MB	PC-133	16Mx16	8	2	N

4. Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	GND	85	GND	29	DM1	113	DM5	57	D18	141	D50
2	D0	86	D32	30	CS0-	114	CS1-	58	D19	142	D51
3	D1	87	D33	31	DU	115	RAS-	59	VCC	143	VCC
4	D2	88	D34	32	GND	116	GND	60	D20	144	D52
5	D3	89	D35	33	A0	117	A1	61	NC	145	NC
6	VCC	90	VCC	34	A2	118	A3	62	V_{REF} (3)	146	V_{REF} (3)
7	D4	91	D36	35	A4	119	A5	63	CKE1	147	NC
8	D5	92	D37	36	A6	120	A7	64	GND	148	GND
9	D6	93	D38	37	A8	121	A9	65	D21	149	D53
10	D7	94	D39	38	A10	122	BA0	66	D22	150	D54
11	D8	95	D40	39	BA1	123	A11	67	D23	151	D55
12	GND	96	GND	40	VCC	124	VCC	68	GND	152	GND
13	D9	97	D41	41	VCC	125	CK1	69	D24	153	D56
14	D10	98	D42	42	CK0	126	A12	70	D25	154	D57
15	D11	99	D43	43	GND	127	GND	71	D26	155	D58
16	D12	100	D44	44	DU	128	CKE0	72	D27	156	D59
17	D13	101	D45	45	CS2-	129	CS3-	73	VCC	157	VCC
18	VCC	102	VCC	46	DM2	130	DM6	74	D28	158	D60
19	D14	103	D46	47	DM3	131	DM7	75	D29	159	D61
20	D15	104	D47	48	DU	132	A13	76	D30	160	D62
21	CB0 (2)	105	CB4 (2)	49	VCC	133	VCC	77	D31	161	D63
22	CB1 (2)	106	CB5 (2)	50	NC	134	NC	78	GND	162	GND
23	GND	107	GND	51	NC	135	NC	79	CK2	163	CK3
24	NC	108	NC	52	CB2 (2)	136	CB6 (2)	80	NC	164	NC
25	NC	109	NC	53	CB3 (2)	137	CB7 (2)	81	NC	165	SA0
26	VCC	110	VCC	54	GND	138	GND	82	SDA	166	SA1
27	WE-	111	CAS-	55	D16	139	D48	83	SCL	167	SA2
28	DM0	112	DM14	56	D17	140	D49	84	VCC	168	VCC

(1) NC = No Connect, DU = Reserved for Future Use.
(2) CB0~CB7 is for x72 Unbuffered DIMM/wECC.
(3) VREF is power supply for reference.

5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A12	SDRAM address bus	CKE0 – CKE1	SDRAM clock enable lines
SA0 - SA1	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS-	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS-	SDRAM column address strobe	DQM0 – DQM7	SDRAM data masks
WE-	SDRAM write enable	V_{DD}	Power Supply
CS0- - CS1-	Chip select input	GND	Ground
CLK0 – CLK1	SDRAM Clock input.	DU	Spare Pin
D0 – D63	DIMM memory data bus	NC	No connection

6. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
T_{STG}	Storage Temperature	-55 to 125	°C
V_{INPUT}	Voltage input pins relative to Vss	-1.0 to +4.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +4.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-1.0 to +4.6	V

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7. DC Operating Conditions

- DC Electrical Operating Conditions

(T_A = 0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
VDD	Supply Voltage	3.0	3.3	3.6	V	1
VDDQ	Supply Voltage	3.0	3.3	3.6	V	1
VIH (DC)	Input High (Logic1) Voltage	2.0	-	VCC + 0.3	V	1,2
VIL (DC)	Input Low (Logic0) Voltage	-0.5	-	0.8	V	1,3

Note:

1. All voltages referenced to Vss and VssQ
2. **VIH (max) = VDD** + 1.2V for pulse width ≤ 5ns.
3. **VIL (min) = VSS** +-1.2V for pulse width ≤ 5ns.

- DC Electrical Characteristics

(T_A = 0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
II(L)	Input Leakage Current, any input (0.0V ≤ VIN ≤ VDD), All Other Pins Not Under Test = 0V	-10	+10	µA
IO(L)	Output Leakage Current (DOUT is disabled, 0.0V ≤ VOUT ≤ VDDQ)	-10	+10	µA
VOH	Output Level (LVTTL) Output “H” Level Voltage (IOUT = -2.0mA)	2.4	-	V
VOL	Output Level (LVTTL) Output “L” Level Voltage (IOUT = +2.0mA)	-	0.4	V

8. Capacitance

(T_A = 0 ℃ ~ 70 ℃; V_{DD} = 3.3±0.3V)

Symbol	Parameter	Max	Units
C_{I1}	Input Capacitance (A0 to A11, /RAS,/CAS, /WE)	40	pF
C_{I2}	Input Capacitance (/CS0, /CSI)	25	pF
C_{ICL}	Input Capacitance (CLK0-CLK1)	28	pF
C_{I3}	Input Capacitance (CKE0, CKEI)	20	pF
C_{I4}	Input Capacitance (DQ0-DQ7)	10	pF
C_{SC}	Input Capacitance (SCL, SA0-2)	8	pF
C_{IO}	Input/Output Capacitance	18	pF

9. Operating, Standby, and Refresh Currents

- 256MB UDIMM (2 Ranks, 16Mx16 SDR SDRAMs T_A = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter/Condition		PC-133	Unit
I_{CC1}	Operation Current: Burst length = 4, CL = 3, t_{RC}> = t_{RC}(min), t_{CK}> = t_{CK}(min), IO = 0 mA, 2 Bank Interleave Operation		1015	mA
I_{CC2P}	Precharged Standby Current in Power Down Mode: CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)		40	mA
I_{CC2N}	Precharged Standby Current in Non-Power Down Mode: CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed once in 3 cycles.		315	mA
I_{CC3N}	Active Standby Current in Non-Power Down Mode: CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed one time		315	mA
I_{CC3P}	Active Standby Current in Power Down Mode: CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)		75	mA
I_{CC4}	Burst Operating Current: Burst length = Full Page, t_{RC} = Infinite, CL = 3, t_{CK}> = t_{CK}(min), IO = 0 mA 2 Banks Activated		1090	mA
I_{CC5}	Auto Refresh Current: t_{RC}>= t_{RC}(min)		4300	mA
I_{CC6}	Self Refresh Current: CKE = <0.2 V	Standard	30	mA
		L-Version	20	

1. Currents given are valid for a single device. .
2. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC}(min).
3. The specified values are obtained with the output open.
4. Input signals are changed once during t_{CK}(min).
5. Input signals are changed once during three clock cycles.
6. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7. Input signals are stable.

10. AC Timing Specifications

(T_A =0 °C ~ 70 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC-133		Unit
		Min.	Max.	
Clock and Clock Enable				
tAC	DQ output access time from CK/CK#	-	5.4	ns
tCH	CK high-level width	2.5	-	ns
tCL	CK low-level width	2.5	-	ns
fCK	System frequency	100	133	MHz
tCK	Clock Cycle Time	7.5	10	ns
tCS	input setup time	1.5	-	ns
tCH	input hold time	0.8	-	ns
tCKSP	CKE Setup Time (Power down mode)	2	-	ns
tCKSR	CKE Setup Time (Self Refresh Exit)	8	-	ns
tT	Transition time (rise and fall)	1	-	ns
Command Parameters				
tRCD	/RAS to /CAS delay	20	-	ns
tRC	Cycle Time	60	-	ns
tRAS	Active command Period	45	100K	ns
tRP	Precharge Time	20	-	ns
tRRD	Bank to Bank delay time	15	-	ns
tCCD	/CAS to /CAS delay time (same bank)	1	-	CLK
Refresh Cycle				
tSREX	Self Refresh Exit Time	10	-	ns
tREF	Refresh Period (8192 cycles)	64	-	ms

Symbol	Parameter	PC-133		Unit
		Min.	Max.	
Read Cycle				
tOH	Data Out Hold Time	3	-	ns
tLZ	Data Out to Low Impedance Time	0	-	Ns
tHZ	Data Out to High Impedance Time	3	7.5	ns
tDQZ	DQM Data Out Disable Latency	2	-	CLK
Write Cycle				
tDPL	Data input to Precharge (write recovery)	1	-	CLK
tDAL	Data In to Active/refresh	5	-	CLK
tDQW	DQM Write Mask Latency	0	-	CLK

11. SPD

Serial Presence Detect – (256MB)

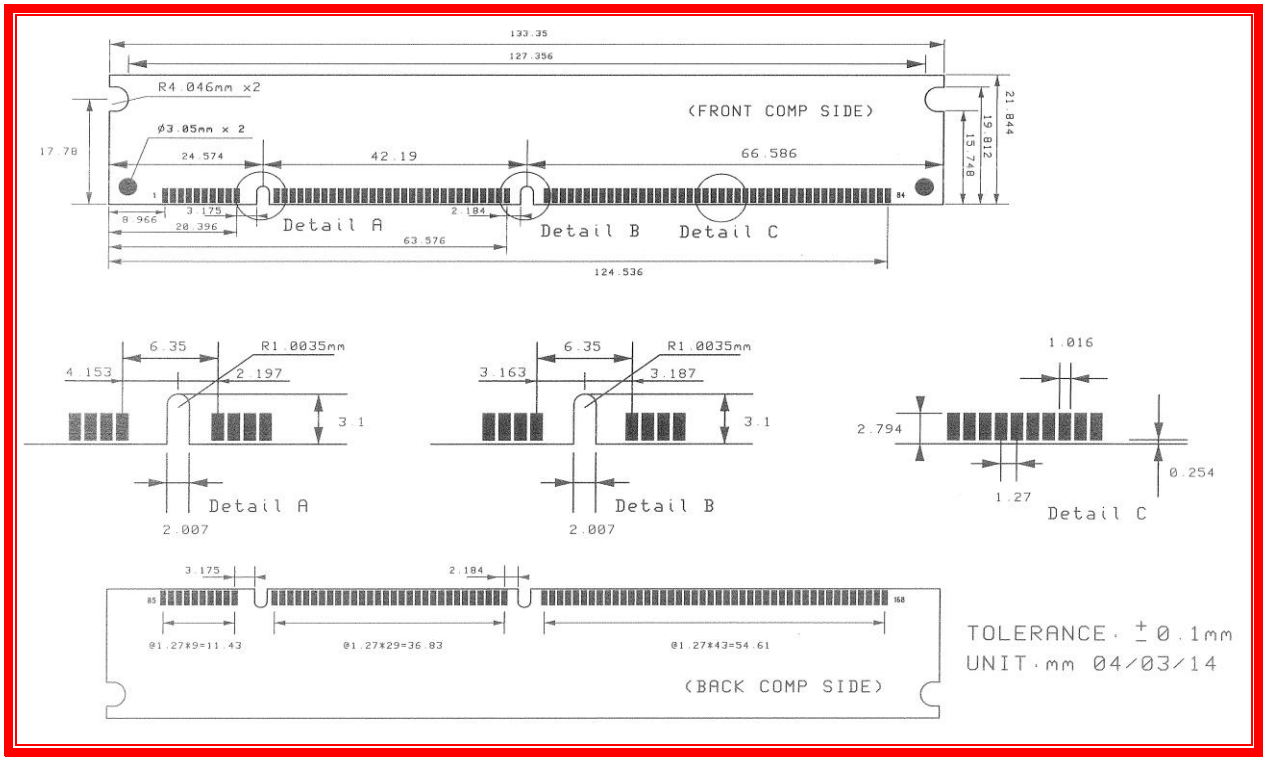
16Mx64 2 RANKs UNBUFFERED SDRAM DIMM based on 16Mx16, 4Banks, 8K Refresh, with SPD

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	80	
1	Total Number of Bytes in Serial PD device	08	
2	Fundamental Memory Type	04	
3	Number of Row Addresses on Assembly	0D	
4	Number of Column Addresses on Assembly	09	
5	Number of DIMM Bank, Package, and Height	02	
6	Data Width of this Assembly	40	
7	Reserved	00	
8	Voltage Interface Level of this Assembly	01	
9	DDR2 SDRAM Cycle Time at CL=5 (ns)	75	
10	DDR2 SDRAM Access Time from Clock at CL=5 (ns)	54	
11	DIMM Configuration Type	00	
12	Refresh Rate/Type	82	
13	Primary DDR2 SDRAM Width	10	
14	Error Checking DDR2 SDRAM Device Width	00	
15	Minimum Clock Delay from Back to Back Random Column Address	01	
16	Burst Length Supported	8F	
17	Number of Device Banks	04	
18	/CAS Latencies Supported	06	
19	/CS Latencies	01	
20	/WE Latencies	01	
21	SDRAM Module Attributes:	00	

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
22	SDRAM Device Attributes: General	0E	
23	Minimum Clock Cycle at CL=2	A0	
24	Maximum Data Access Time (t_{ac}) from Clock at CL=2	60	
25	Minimum Clock Cycle Time at CL=1	00	
26	Maximum Data Access Time (t_{ac}) from Clock at CL=1	00	
27	Minimum Row Precharge Time (t_{RP})	14	
28	Minimum Row Active to Row Active delay (t_{RRD})	0F	
29	Minimum RAS to CAS delay (t_{RCD})	14	
30	Minimum RAS Pulse Width (t_{RAS})	2D	
31	Module Bank Density	20	
32	SDRAM Input Setup Time	15	
33	SDRAM Input Hold Time	08	
34	Data Input Setup Time Before Clock (t_{DS})	15	
35	Data Input Hold Time After Clock (t_{DH}) (ns)	08	
36-48	Superset Information (May be used in Future)	00	
49	Reserve	00	
50-61	Reserve	00	
62	SPD Revision	02	
63	Checksum for Bytes 0 - 62	AA	
64-71	Manufacture's JEDEC ID Code	**7F 7F 7F 7F 7F 7F F1 FF**	
72	Module Manufacturing Location	**02**	
73-91	Module Part number	**69 2D 44 49 4D 4D 4D FF FF FF FF FF FF FF FF FF FF FF FF 00**	
92-255	Reserved	**-**	

12. PACKAGE DIMENSION

- (256M, 2 Ranks, 16Mx16 SDR SDRAMs)



Note: Device position is only for reference.

13. RoHS Declaration

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Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M0UB-56PA1C03/-(X) complies with the requirement of RoHS directives 2006/12/EC

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI（Cr+6）	< 1000 ppm
Polybromodiphenyl ether（PBDE）	< 1000 ppm
Polybrominated Biphenyls（PBB）	< 1000 ppm

Date issued: 2013/07/23

Manufacturer: ： InnoDisk Co., Ltd.
Address：9F, No. 100, Sec.1 Xintai 5th Rd., Xizhi City, Taipei 221, Taiwan

Authorized Signature：

QA Dept. Director – Ryan Tsai

Revision Log

Rev	Date	Modification
0.1	24th December 2013	Preliminary Edition
1.0	9th April 2014	Official Release.