L506 Hardware Design

LTE Module Series

Version： V1.4

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Shanghai Mobiletek Communication Ltd

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Version History

Date	Version	Description of change	Author
2016-03-09	V1.0	Initial	
2016-06-02	V1.1		
2016-06-25	V1.2		
2016-06-28	V1.3	Fixed error picture	
2016-06-29	V1.4	Update rf parameter	

Contents

1 About this document

1.1Applicable scope

This document describes the 4G LTE LCC Module (hereinafter referred to as L506), the basic specifications, product electrical characteristics, design guidance and hardware interface development guidance. Users need to follow this documentation requirements and guidance for design.

This document applies only to L506 products in the application development.

1.2 Writing purpose

This document provides the design and development basis for the product users. By reading this document, users can have a whole understanding of the product, the technical parameters of the product have a clear understanding, and can be used in this document to complete the development of wireless 4G Internet access functions.

This hardware development document not only provides the product functional features and technical parameters, but also provides product reliability testing and related testing standards, business functions to achieve process, RF performance indicators and user circuit design guidance.

1.3 Support and reference documents list

In addition to the hardware development documentation, we also provide a guide to the development board based on this product manual and software development instruction manual, 1-1 is supported as a list.

Table 1-1 support document list

No.	Documents
1	《L506 AT Command User Guide》
2	《L506_SPEC_1604.docx》
3	《L506 EVB User Manual》
4	《L506 Schematic checklist》
5	《L506 Layout checklist》
6	《L506_Reference Design_V3.pdf》

7	《L506_V3_DECAL.sch》
8	《L506_V3_DECAL.PCB》

1.4 Terms and Abbreviations

Table 1-2 is the Document relative Terms and Abbreviations。

Table 1-1 Terms and Abbreviations

Abbreviation	Descriptions
ESD	Electro-Static discharge
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver Transmitter
SDCC	Secure Digital Card Controller
USIM	Universal Subscriber Identification Module
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit
PCM	Pulse-coded Modulation
I/O	Input/output
LED	Light Emitting Diode
GPIO	General-purpose Input/Output
GSM	Global Standard for Mobile Communications
GPRS	General Packet Radio Service
WCDMA	Wideband Code Division Multi Access
UMTS	Universal Mobile Telecommunication System
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
AGPS	Assisted Global Positioning System
BER	Bit Error Rate
DL	Downlink
DPCH	Dedicated Physical Channel
DPCH_Ec	Average energy per PN chip for DPCH. DPCH

2 Product Overview

L506 Designed for global market, L506 supports 5 air-interface standards include GSM, TD-SCDMA, CDMA, WCDMA and LTE. User can choose the module based on the wireless network configuration. In this document, the supported radio band is described in the following items. This product is a LCC interface of 4G wireless internet module, with the high speed, small size, light weight, high reliability can be widely used in various products and devices with wireless internet access:

- Four-Band TDD-LTE B38/B39/B40/B41
- Five-Band FDD-LTE B1/B3/B7/B8/(B20)
- Dual-Band TD-SCDMA B34/B39
- Dual-Band UMTS/HSDPA/HSPA+ B1/B8
- GSM/GPRS/EDGE 900/1800 MHz
- GPS/BEIDOU/GLONASS
- AGPS

Data transmission specifications

- LTE

- Uplink up to 50Mbps,
- Downlink up to 150Mbps

- TD-HSDPA/HSUPA

- Uplink up to 2.2 Mbps,
- Downlink up to 4.2 Mbps

- TD-SCDMA

- Uplink up to 128Kbps,
- Downlink up to 384Kbps

- HSPA+

- Uplink up to 5.76 Mbps,
- Downlink up to 42 Mbps

- UMTS

- Uplink/Downlink up to 384Kbps

- EDGE Class:

- Max. 236.8Kbps(DL),Max. 236.8Kbps(UL)

- GPRS

- Max. 85.6Kbps(DL), Max. 85.6Kbps(UL)

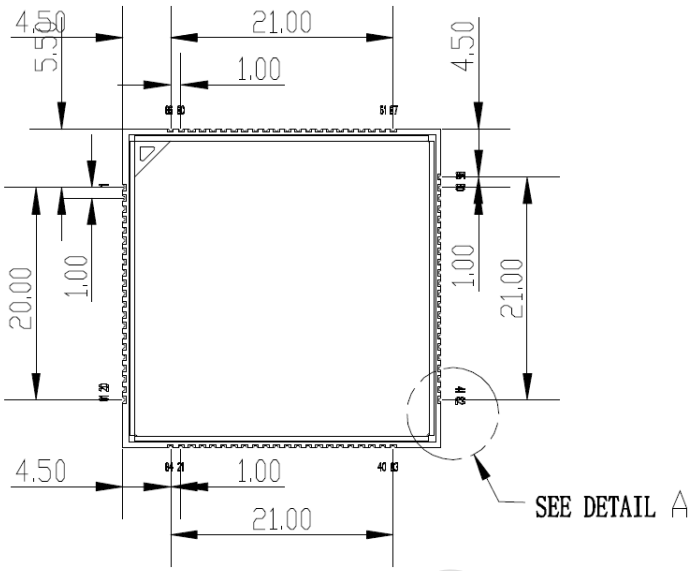
- Support SMS;
- Support dual voltage USIM interface(3.0V/1.8V); USB2.0 interface UART、keypad、GPIO、PCM etc;
- Can provide mobile environment GSM/GPRS/EDGE, UMTS/HSDPA+/TD-HSDPA /HSUPA/LET high-speed data access services;
- Dimensions（L×W×H）:30mm×30mm×2.8mm

TOP VIEW BOTTOM VIEW

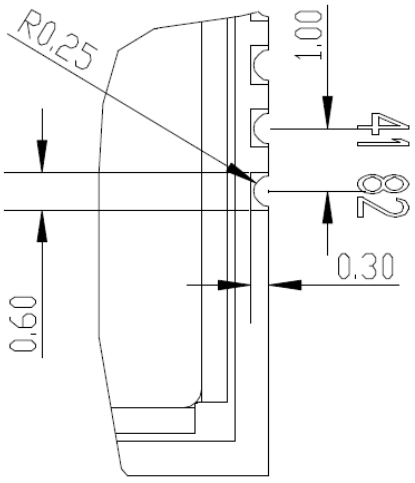
Figure 2-1 Product Physical Map

2.1 Package Dimensions

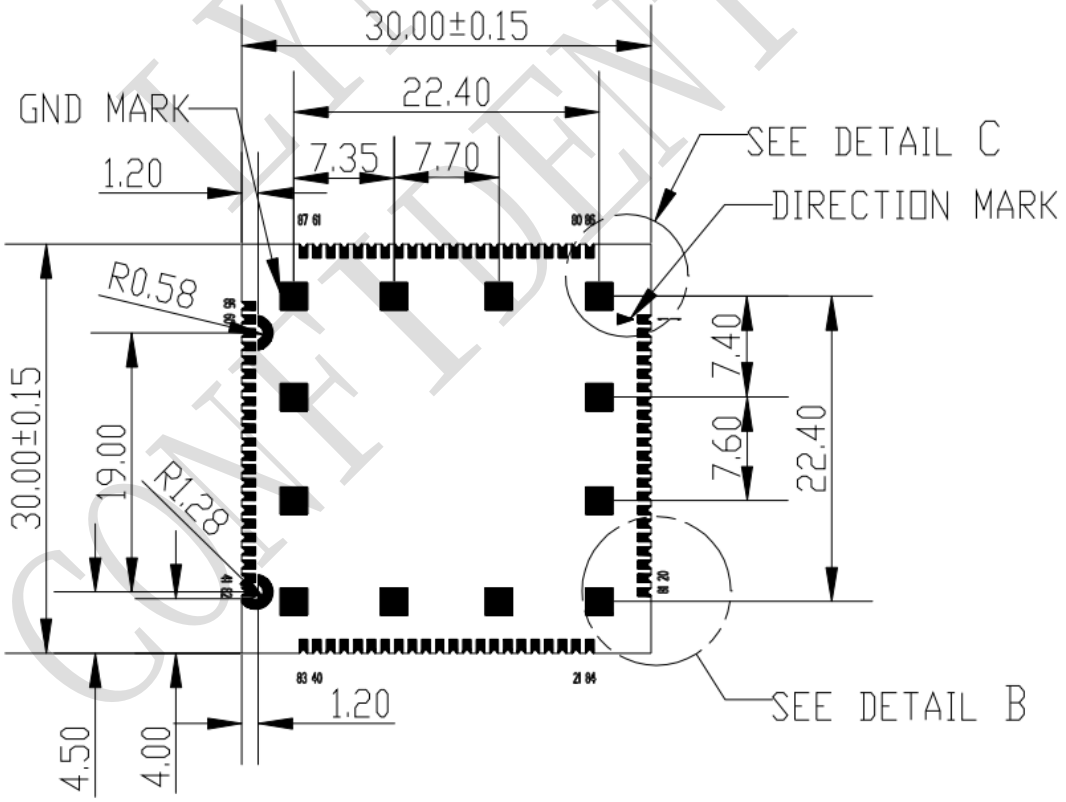
The product module is 87-PIN LCC package module, in addition to signal pin, also contains many special heat welding disc to improve joint performance, mechanical strength and heat dissipation performance, the heat release welding disc 12 and uniform distribution in the bottom of the PCB. Package size is 30 x 30 mm, the height is 2.8 mm. Pin 1 position from the bottom of the belt angle welding plate to identify, the missing corner where the direction of the corresponding module angle pad, figure 2-2 is the product dimension type map:



(a)Top Dimensions (Unit mm)

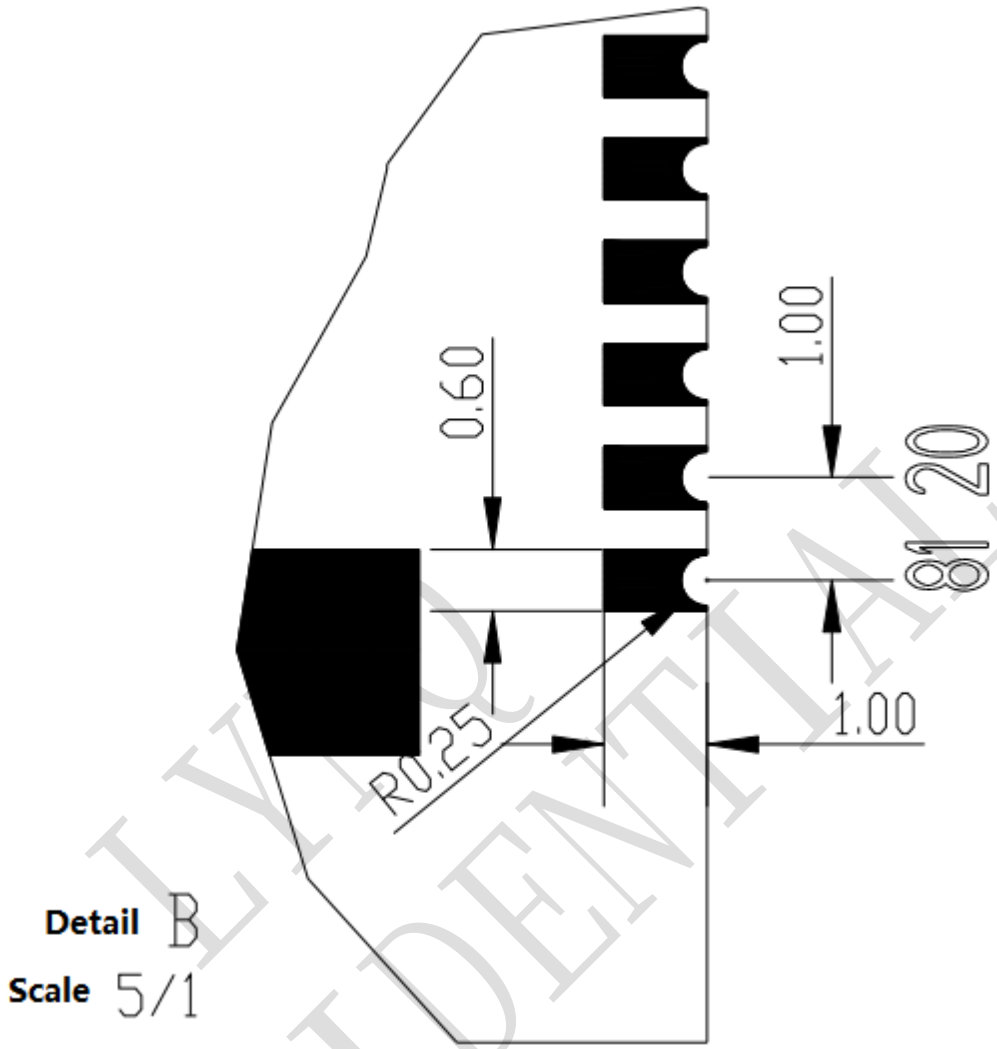


(b)Top Detail (Unit mm)A

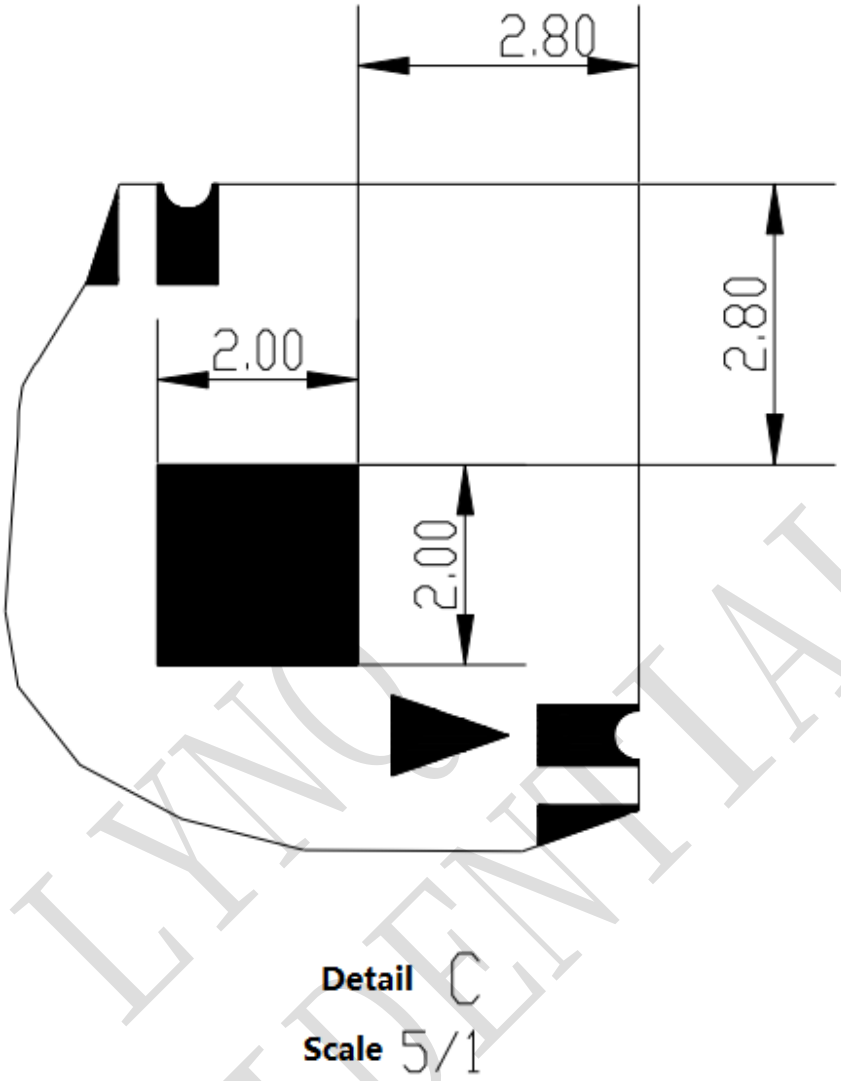


(c)Bottom Dimensions (Unit mm)

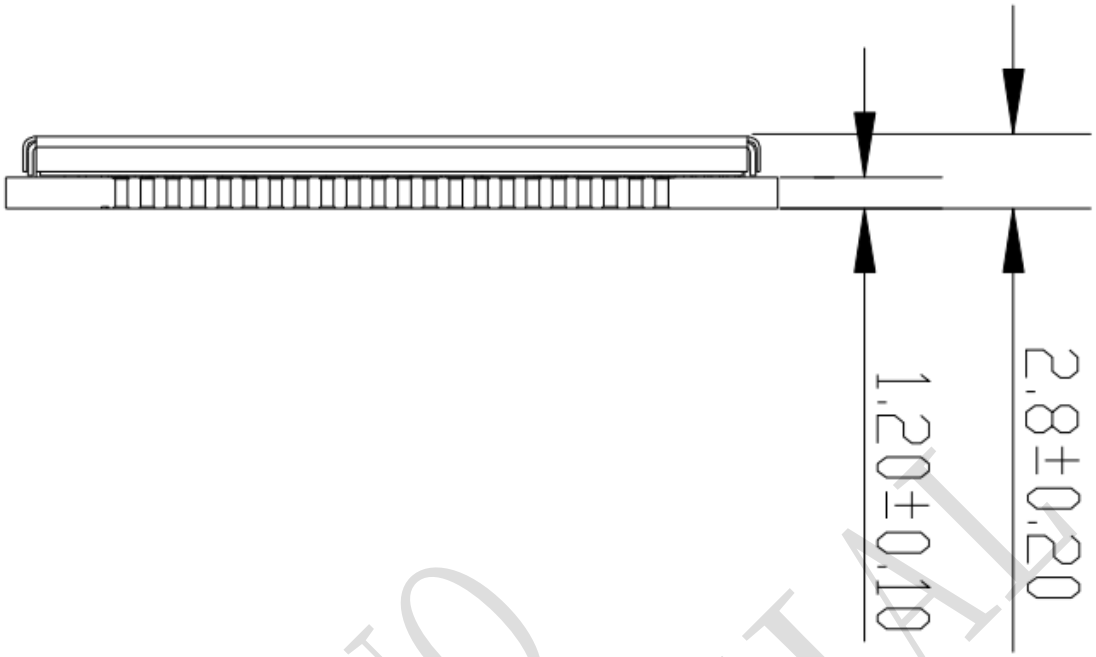
Note: antenna feed point in actual use of the customers don't need (PCB assembly, the stencil file).



(d)Bottom Detail B (Unit mm)



(e)Bottom Detail C (Unit mm)



(e)Side view Dimensions(Unit mm)

Figure 2-2 Module Dimensions

2.2 Product Function Outline

2.2.1 Hardware Diagram

This product mainly includes the following signal group：USB Interface signal、USIM card Interface signal、I2C Interface signal、UART Interface signal、PCM Interface signal、UART Interface signal、JTAG Interface signal、SPI interface、Module startup、Module control signal、Power supply and ground. The global architecture of the L506 module is described in the figure below.

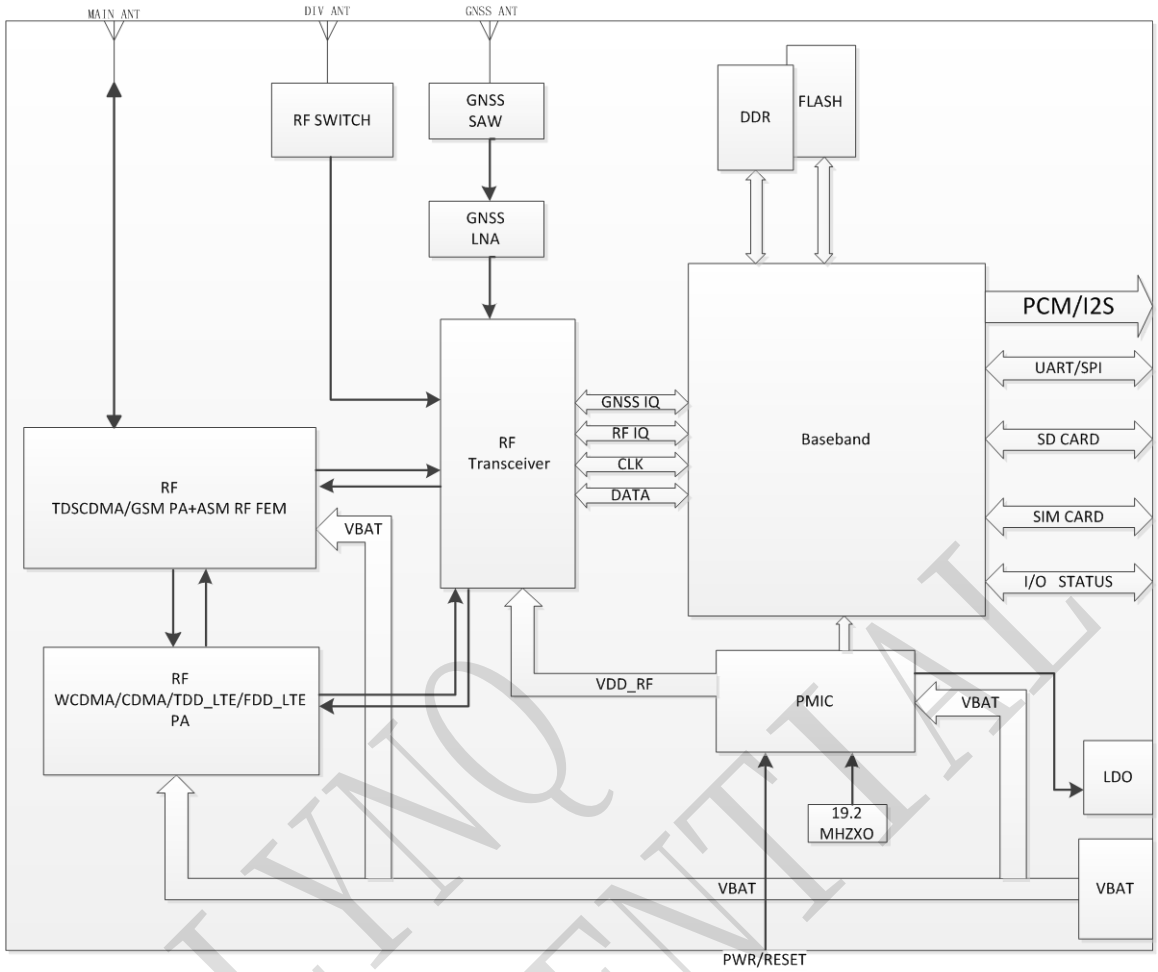


Figure 2-1 L506 System Functional Architecture

2.2.2 Radio frequency function

RF Function Overview:

- Four-Band TDD-LTE B38/B39/B40/B41
- Five-Band FDD-LTE B1/B3/B7/B8/B20
- Dual-Band TD-SCDMA B34/B39
- Dual-Band UMTS/HSDPA/HSPA+ B1/B8
- GSM/GPRS/EDGE 900/1800 MHz
- GPS/BEIDOU/GLONASS

The operating frequency range of the transmitter is shown in table 2-2.

Table 2-2 RF frequency band

Working band	Upstream band（Uplink）	Downlink frequency（Downlink）
UMTS900	890 MHz — 915MHz	925 MHz — 960 MHz
UMTS1900	1850 MHz — 1910 MHz	1930 MHz — 1990 MHz
GSM900	890 MHz — 915MHz	925 MHz — 960MHz
GSM1800	1710 MHz — 1785MHz	1805 MHz — 1880MHz
TD-SCDMA B34	2010～2025 MHz	2010～2025 MHz

TD-SCDMA B39	1880～1920 MHz	1880～1920 MHz
TDD_LTE B38	2570 MHz~2620 MHz	2570 MHz~2620 MHz
TDD_LTE B39	1880 MHz~1920 MHz	1880 MHz~1920 MHz
TDD_LTE B40	2300 MHz~2400 MHz	2300 MHz~2400 MHz
TDD_LTE B41	2555～2655 MHz	2555～2655 MHz
FDD_LTE B1	1920 MHz~1980 MHz	2110 MHz~2170 MHz
FDD_LTE B3	1710 MHz~1785 MHz	1805 MHz~1880 MHz
FDD_LTE B7	2500 MHz~2570 MHz	2620 MHz~2690 MHz
FDD_LTE B8	880 MHz~915 MHz	925 MHz~960 MHz
FDD_LTE B20	832 MHz~862 MHz	791 MHz~821 MHz
GPS L1 BAND	--	1574.4 ～1576.44 MHz
GLONASS	--	1598 ～1606 MHz
BEIDOU B1	--	1559.05 ～1563.14 MHz

Table 2-3 Conducted transmission power

Working Band	Max Power	Min Power
UMTS900	24dBm +1/-3dB	<-50dBm
UMTS1900	24dBm +1/-3dB	<-50dBm
GSM900	33dBm ±2dB	5dBm ± 5dB
DCS1800	30dBm ±2dB	0dBm ± 5dB
GSM900(8-PSK)	27dBm ±3dB	5dBm ± 5dB
DCS1800(8-PSK)	26dBm +3/-4dB	0dBm ± 5dB
TD-SCDMA B34	24dBm +1/-3dB	<-50dBm
TD-SCDMA B39	24dBm +1/-3dB	<-50dBm
TDD_LTE B38	23dBm +/-2.7dB	<-40dBm
TDD_LTE B39	23dBm +/-2.7dB	<-40dBm
TDD_LTE B40	23dBm +/-2.7dB	<-40dBm
TDD_LTE B41	23dBm +/-2.7dB	<-40dBm
FDD_LTE B1	23dBm +/-2.7dB	<-40dBm
FDD_LTE B3	23dBm +/-2.7dB	<-40dBm
FDD_LTE B7	23dBm +/-2.7dB	<-40dBm
FDD_LTE B8	23dBm +/-2.7dB	<-40dBm
FDD_LTE B20	23dBm +/-2.7dB	<-40dBm

Table 2-4 Conducted receive sensitivity

Working Band	Receive sensitivity(Typical)	Receive sensitivity(MAX)
WCDMA B1	< -109dBm	3GPP
WCDMA B8	< -109dBm	3GPP
GSM900	< -109dBm	3GPP

DCS1800	< -108dBm	3GPP
TD-SCDMA B34	< -110dBm	3GPP
TD-SCDMA B39	< -110dBm	3GPP

Table 2-5 Reference sensitivity (QPSK)

Channel bandwidth							
E-UTRA Band	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex Mode
1	--	--	-100	-97.2	-96.2	-95	FDD
3	-102.2	-99.7	-98	-95	-94.2	-93	FDD
7	--	--	-98	-95	-93.2	-92	FDD
8	-103.2	-101.7	-100.2	-97.2	--	--	FDD
20	--	--	-97	-94	-91.2	-90	FDD
38	--	--	-100	-97	-95.2	-94	TDD
39	--	--	-100	-97	-95.2	-94	TDD
40	--	--	-100	-97	-95.2	-94	TDD
41	--	--	-100	-97	-95.2	-94	TDD

3 Interface Description

3.1 PIN Definition

3.1.1 Pin I/O parameter definition

The I/O parameter definition of the product is shown in table 3-1.

Table 3-1 I/O parameter definitions

Pin attribute symbol	Description
PI	Power input PIN
PO	Power output PIN
AI	Analog input
AIO	Analog signal input/output PIN
I/O	Digital signal input/output PIN
DI	Digital signal input
DO	Digital signal output
DOH	Digital output with high level
DOL	Digital output with low level
PD	Pull down
PU	Pull up
AO	Analog output

3.1.2 Pin Configuration

All hardware interfaces which connect L506 to customers' application platform are through 87 pins pads (Metal half hole). Figure 3-1 is L506 outline diagram.

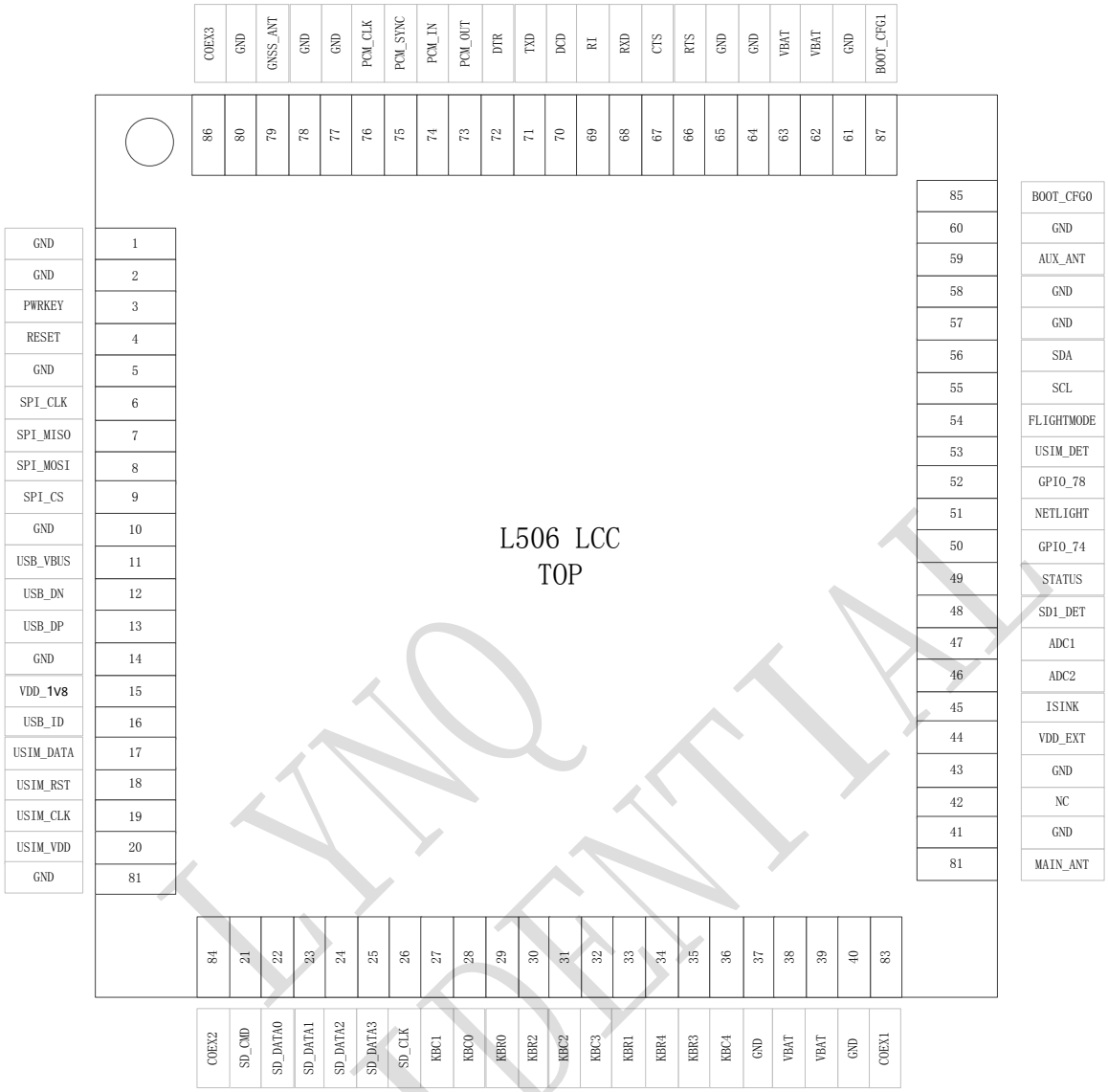


Figure 3-1 **Pin View**(Top View)

3.1.3 PIN Definition and function description

Table 3-2 Pin definition

Pin No.	Define	Pin No.	Define
1	GND	2	GND
3	PWRKEY	4	RESET
5	GND	6	SPI_CLK

7	SPI_MISO	8	SPI_MOSI
9	SPI_CS	10	GND
11	USB_VBUS	12	USB_DN
13	USB_DP	14	GND
15	VDD_1V8	16	USB_ID
17	USIM_DATA	18	USIM_RST
19	USIM_CLK	20	USIM_VDD
21	SD_CMD	22	SD_DATA0
23	SD_DATA1	24	SD_DATA2
25	SD_DATA3	26	SD_CLK
27	KBC1	28	KBC0
29	KBR0	30	KBR2
31	KBC2	32	KBC3
33	KBR1	34	KBR4
35	KBR3	36	KBC4
37	GND	38	VBAT
39	VBAT	40	GND
41	GND	42	NC
43	GND	44	VDD_EXT
45	ISINK	46	ADC2
47	ADC1	48	SD1_DET
49	STATUS	50	GPIO49
51	NETLIGHT	52	GPIO43
53	USIM_DET	54	FLIGHTMODE
55	SCL	56	SDA
57	GND	58	GND
59	AUX_ANT	60	GND
61	GND	62	VBAT
63	VBAT	64	GND
65	GND	66	RTS
67	CTS	68	RXD
69	RI	70	DCD

71	TXD	72	DTR
73	PCM_OUT	74	PCM_IN
75	PCM_SYNC	76	PCM_CLK
77	GND	78	GND
79	GNSS_ANT	80	GND
81	GND	82	MAIN_ANT
83	COEX1	84	COEX2
85	BOOT_CFG0	86	COEX3
87	BOOT_CFG1		

Table 3-3 Pin Function Description

Power interface				
Pin Name	Pin No.	I/O	Description	Content
VBAT	38, 39, 62, 63	PI	Power supply voltage, VBAT=3.4V~4.2V.	The power supply for system Maximum load current must above 2A.
VDD_1V8	15	PO	Module LDO output power ,1.8V output, Max current 150mA, For I/O, MCP, WLAN/BT, SLIC, sensors.	If not use keep it open.
VDD_EXT	44	PO	Module LDO output power, 2.85V output, Max current 300mA.	Only use for external SD Card VDD. If not use keep it open.
GND	1,2,5,10,14,37, 40,41,43,57,58, 60,61,64,65,77, 78,80,81		Ground.	
System Control				
Pin Name	Pin No.	I/O	Description	Content
PWRKEY	47	DI	System power on/off input, active low.	
RESET	38	DI	System reset input, active low.	
FLIGHTMODE	54	DI, PU	The input signal, used to control the system into flight mode, H:	Pull UP to VDD_1V8 (PIN 15) with 10K resistor

			flight mode; L: normal mode	
Module status(GPIO)				
Pin Name	Pin No.	I/O	Description	Content
NETLIGHT	51	DO	Identify the system network status.	
STATUS	40	DO	Module status identify: High level power on, low level power off.	
SD interface				
Pin Name	Pin No.	I/O	Description	Content
SD_CMD	21	DO	SDIO command	Advice add the ESD on you SD card Slot. If not use keep it open
SD_DATA0	22	I/O	SDIO data	
SD_DATA1	23	I/O	SDIO data	
SD_DATA2	24	I/O	SDIO data	
SD_DATA3	25	I/O	SDIO data	
SD_CLK	26	DO	SDIO clock	
SD_CARD_DET_N	48	DI，PU	Default: GPIO26 Optional: Input pin as SD card detecting. H: SD card is removed L: SD card is inserted	L506 have internal pull up, so SD card slot should choose insert detect PIN connect the ground. If not use keep it open
SIM interface				
Pin Name	Pin No.	I/O	Description	Content
USIM_DETECT	53	DI，PU	Default: GPIO34 Optional: Input pin as USIM card detect pin. H: USIM is removed L: USIM is inserted	L506 have internal pull up, If not use keep it open.
USIM_DATA	17	I/O	USIM Card data I/O, which has been pulled up with a 10KR resistor to USIM_VDD in module. Do not pull up or pull down in users' application	All signals of USIM interface should be protected against ESD/EMC.

			circuit.	
USIM_RESET	18	DO	USIM Reset	
USIM_CLK	19	DO	USIM Clock	
USIM_VDD	20	PO	USIM Card Power output, output Voltage depends on USIM mode automatically， and one is 3.0V±10%, another is 1.8V±10%. Current is less than 50mA.	
PCM interface				
Pin Name	Pin No.	I/O	Description	Content
PCM_CLK	76	DO	PCM data bit clock.	If not use keep it open.
PCM_SYNC	75	DO	PCM data frame sync signal.	
PCM_IN	74	DI	PCM data input.	
PCM_OUT	73	DO	PCM data output.	
FULL UART/DEBUG PORT				
Pin Name	Pin No.	I/O	Description	Content
RTS	66	DI	DET Request to send.	If not use keep it open.
CTS	67	DO	Clear to Send.	If not use keep it open.
RX	68	DI	Receive Data.	If not use keep it open.
RI	69	DO	Ring Indicator.	Multiplexed as MDM_DBG_UART_TX, If not use keep it open. Recommend reserved the test point for debug
DCD	70	DO	Carrier detects.	If not use keep it open
TXD	71	DO	Transmit Data.	If not use keep it open.
DTR	72	DI	DTE get ready.	Multiplexed as MDM_DBG_U

				ART_RX, If not use keep it open. Recommend reserved the test point for debug
I2C interface				
Pin Name	Pin No.	I/O	Description	Content
I2C_SCL	55	DO	I2C clock output.	L506 internal have pulled up to 1.8V
I2C_SDA	56	I/O	I2C data input/output.	
Keypad interface				
Pin Name	Pin No.	I/O	Description	Content
KBR0	29	DOH	Bit 0 drive to the pad matrix	All Keypad pins can be configured as GPIOs. If not use keep it open.
KBR1	33	DOH	Bit 1 drive to the pad matrix	
KBR2	30	DOH	Bit 2 drive to the pad matrix	
KBR3	35	DOH	Bit 3 drive to the pad matrix	
KBR4	34	DOH	Bit 4 drive to the pad matrix	
KBC0	28	DI, PD	Bit 0 for sensing key press on pad matrix	
KBC1	27	DI, PD	Bit 1 for sensing key press on pad matrix	
KBC2	31	DI, PD	Bit 2 for sensing key press on pad matrix	
KBC3	32	DI, PD	Bit 3 for sensing key press on pad matrix	
KBC4	36	DI, PD	Bit 4 for sensing key press on pad matrix	
GPIO				
Pin Name	Pin No.	I/O	Description	Content
GPIO_74	50	I/O	Default: GPIO Optional: Input pin as wake/interrupt signal to module from host.	If not use keep it open.
NC/GPIO78	52	DO	NC or for external	

			tuner(B12,B17,B28) control pin	
NC/GPIO45	42	DO	Default GPIO_45 or for external tuner(B12, B17,B28) control pin.	
ISINK	45	DO	Used to control external for current sink.	
RF port				
Pin Name	Pin No.	I/O	Description	Content
MAIN _ANT	82	AIO	Main Antenna	
AUX_ANT	59	AI	diversity antenna	
GNSS_ANT	79	AI	GPS antenna	
Others				
Pin Name	Pin No.	I/O	Description	Content
ADC1	47	AI	Analog conversion digital input interface1	If not use keep it open.
ADC2	46	AI	Analog conversion digital input interface2	
COEX1	83	I/O	RF synchronizing between wifi and LTE.	If not use keep it open.
COEX3	86	I/O		
COEX2	84	I/O	Default: RF synchronizing between wifi and LTE. Optional: Pull up to 1.8V(L506 PIN 15 VDD_1V8) with 10K resistor force module in USB download mode	Recommend placing test points for debug.
BOOT_CFG0	85	DI, PD	Pull up to 1.8V(L506 PIN 15 VDD_1V8) with 10K resistor force module in fastboot mode	
BOOT_CFG1	87	DI, PD	Pull up to 1.8V(L506 PIN 15 VDD_1V8) with	

			10K resistor force module in fastboot mode	

3.2 Electrical Specifications

3.2.1 Absolute maximum ratings

Table 3-4 module absolute maximum ratings

Parameter	Min.	Max.	Unit
Voltage at VBAT	0.5	6.0	V
Voltage at USB_VBUS	-0.5	5.25	V
Voltage at digital pins (PWRKEY,RESET,SPI,Keypad,GPIO,I2C,UART,PCM)	-0.3	2.1	V
Voltage at digital pins (SD,USIM)	-0.3	3.05	V

3.2.2 Operating conditions

Table 3-4 module recommended operating condition

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Main power supply for the module	3.4	3.8	4.2	V
USB_VBUS	Voltage at USB_VBUS	2.0	5.0	5.25	V

3.3 Digital I/O characteristics

Table 3-5 1.8V Digital I/O characteristics

Parameter	Description	Min.	Min.	Max.	Unit
VIH	High level input voltage	0.7*VDD_PX	0.7*VDD_PX	VDD_PX+0.3	V
VIL	Low level input voltage	-0.3	-0.3	0.2* VDD_PX	V
VOH	High level output voltage	VDD_PX-0.45	VDD_PX-0.45	VDD_PX	V

VOL	Low level output voltage	0	0	0.45	V
IOH	High-level output current (no pull down resistor)	-	2	-	mA
IOL	Low-level output current (no pull up resistor)	-	-2	-	mA
IIH	Input high leakage current (no pull down resistor)	-	-	1	uA
IIL	Input low leakage current (no pull up resistor)	-1	-	-	uA

Note: These parameters are for digital interface pins, such as SPI, Keypad, GPIOs (NETLIGHT, FLIGHTMODE, STATUS, USIM_DET, SD1_DET), I2C, UART, PCM, COEXn, BOOT_CFGn.

3.4 Power Interface

3.4.1 Power supply pin description

Table 3-6 DC Power Characteristics

Pin No.	Net Name	Description	DC Characteristic (V)		
			Min.	Typ.	Max.
38, 39, 62, 63	VBAT	Power supply for the module	3.4	3.8	4.2
1, 2, 5, 10, 14, 37, 40, 41, 43, 57, 58, 60, 61, 64, 65, 77, 78, 80, 81	GND	GND	-	-	-
44	VCC_EXT	Power supply for external SD card	-	2.85	-
20	USIM_VDD	Power supply for VDD SIM	-	1.8/3.0	-
15	VDD_1V8	LDO 1.8V output	-	1.8	-
88-99*	GND	Thermal and welding fixed plate	-	-	-

Note: Pin88~Pin99 (total12pin) is design for the thermal welding fixed plate.

3.4.2 Power supply requirements

There are four VBAT PIN power for the module, VBAT directly power supply for the module baseband and PA, and operating rating is 3.4V~4.2V; In the weak network environment, the antenna will be maximum power emission. The peak current of the module under the 2G mode may reach the peak current of 1.8A. power supply to reach 2A, the average current to reach 0.9A above. Due to the launch of GSM/GPRS time slot pulse can cause VBAT power source instantaneous voltage drop, maximum peak current can reach 2A, So the max power supply current must more than 2 A. Figure 3-2 sign for GSM/GPRS instantaneous pulse diagram.

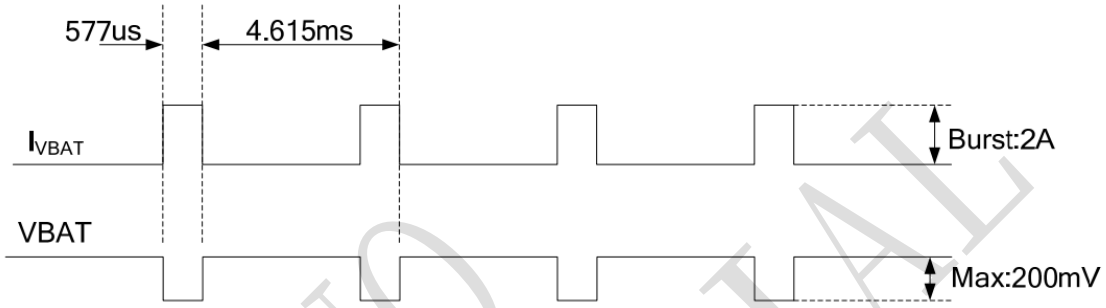


Figure 3-2 GSM/GPRS instantaneous pulse

Table 3-7 VBAT power supply interface characteristics

Symbol	Description	Min	Typ	Max	Unit
VBAT	Power supply voltage	3.4	3.8	4.2	V
IVBAT(peak)	Power supply p current	-	2*	-	A
IVBAT(average)	Power supply average current	1	1.5	-	A
IVBAT(power-off)	Power supply current in power off mode	-	-	20	uA
IVBAT(power-save)	Power supply current in power save mode(sleep mode)	-	-	5	mA

3.4.3 Power Supply Design Guide

Make sure that the input voltage at the VBAT pin will never drop below 3.4V even during a transmit burst when the current consumption rises up to more than 2A. If the power voltage drops below 3.4V, the RF performance of module may be affected. Using large tantalum capacitors (above 300uF) will be the best way to reduce the voltage drops. If the power current cannot support up to 2A, users must introduce larger capacitor (typical 1000uF) to storage electric power. For the consideration of RF performance and system stability, some multi-layer ceramic chip (MLCC) capacitors (0.1/1uF) need to be used for EMC because of their low ESR in high frequencies. Note that capacitors should be put beside VBAT pins as close as possible. Also User should keep VBAT net wider than 2 mm to minimize PCB trace impedance on circuit board. The following figure is the recommended circuit.

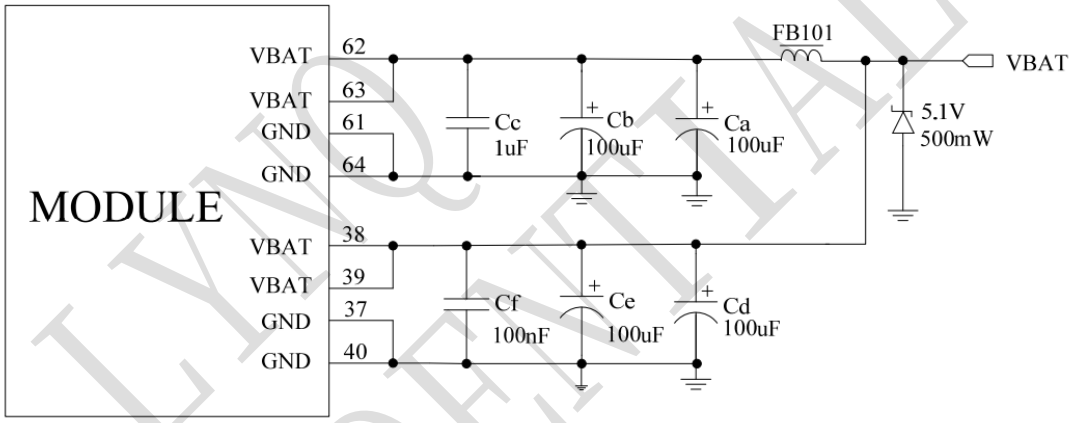


Figure 3-3 VBAT input application circuit

Note: The Cd, Ce, Cb, Cc and Cf are recommended being mounted for L506, but the Ca, Cb, Ce, Ccand Cf for tune.

In addition, in order to get a stable power source, it is suggested to use a Zener diode of which reverse Zener voltage is 5.1V and dissipation power is more than 500mW.

Table 3-7: Recommended Zener diode models

NO.	Manufacturer	Part Number	Power	Package
1	On semi	MMSZ5231BT1G	500mW	SOD123
2	Prisemi	PZ3D4V2H	500mW	SOD123
3	Vishay	MMSZ4689-V	500mW	SOD123
4	Crownpo	CDZ55C5V1SM	500mW	0805

3.4.4 Recommended Power supply circuit

If the voltage difference is not big,We recommend DCDC or LDO is used for the power supply of the module, make sure that the peak current of power components can rise up to more than 2A. The following figure is the reference design of +5V input linear regulator power supply. The designed output for the power supply is 3.8V.

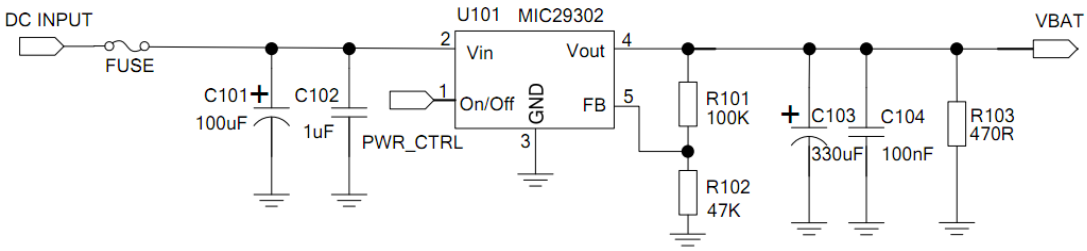


Figure 3-4 **Reference circuit of the LDO power supply**

If there is a big difference between the input voltage and the desired output (VBAT) or better efficiency is more important, a switching converter power supply will be preferable. The following figure is the reference circuit.

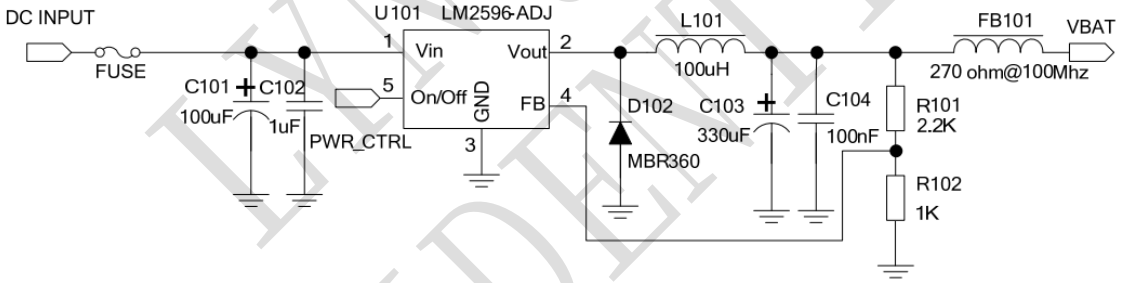


Figure 3-5 **Reference circuit of the DCDC power supply**

Note: DCDC may deprave RF performance because of ripple current intrinsically.

3.4.5 Power Supply Layout guide

The layout of the power supply section and the related components is of vital importance in the power module design. If processes this part layout is not good, will lead to various effects, such as bad EMC, effective the emission spectrum and receiving sensitivity, etc. So the power supply part design is very important, when you design this part you should notes below contents: 1. DC DC switch power should place away from the antenna and other sensitivity circuit; 2. Consider the voltage drop and the module current requirement, the layout line should better above 100mil. If conditions allow should add a power shape plane.

3.5 USIM interface

3.5.1 Pin definition

The USIM provides the required subscription verification information to allow the mobile equipment to attach to a GSM or UMTS network. Both 1.8V and 3.0V SIM Cards are supported.

Table 3-8 USIM Electronic characteristic in 1.8V mode (USIM_VDD =1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	LDO power output	1.75	1.8	1.95	V
V_{IH}	High-level input voltage	0.65·USIM_VDD	–	USIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.35·USIM_VDD	V
V_{OH}	High-level output voltage	USIM_VDD -0.45	––	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

Table 3-9: USIM Electronic characteristic 3.0V mode (USIM_VDD =2.95V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
USIM_VDD	LDO power output	2.75	2.95	3.05	V
V_{IH}	High-level input voltage	0.65*USIM_VDD	–	USIM_VDD +0.3	V
V_{IL}	Low-level input voltage	-0.3	0	0.25·USIM_VDD	V
V_{OH}	High-level output voltage	USIM_VDD -0.45	–	USIM_VDD	V
V_{OL}	Low-level output voltage	0	0	0.45	V

3.5.2 Design Guide

USIM(PIN:17,18,19,20），USIM electronic characteristics as the table 3-8,3-9 show.

In order to meet the 3 GPP TS 51.010 1 protocol and EMC certification requirements. Suggest USIM slot near the location of the module USIM card interface, to avoid running for too long, lead to serious deformation of waveform and effect signal integrity, USIM_CLK and USIM_DATA signal lines suggest ground protect. Between the USIM VCC & GND add a 1uF and a 33 pF capacitor in parallel, Between the USIM_CLK& GND, USIM_RST& GND, USIM DATA& GND add a 33 pF

capacitor in parallel, for filter the RF signal interference.

3.5.3 USIM interface reference circuit

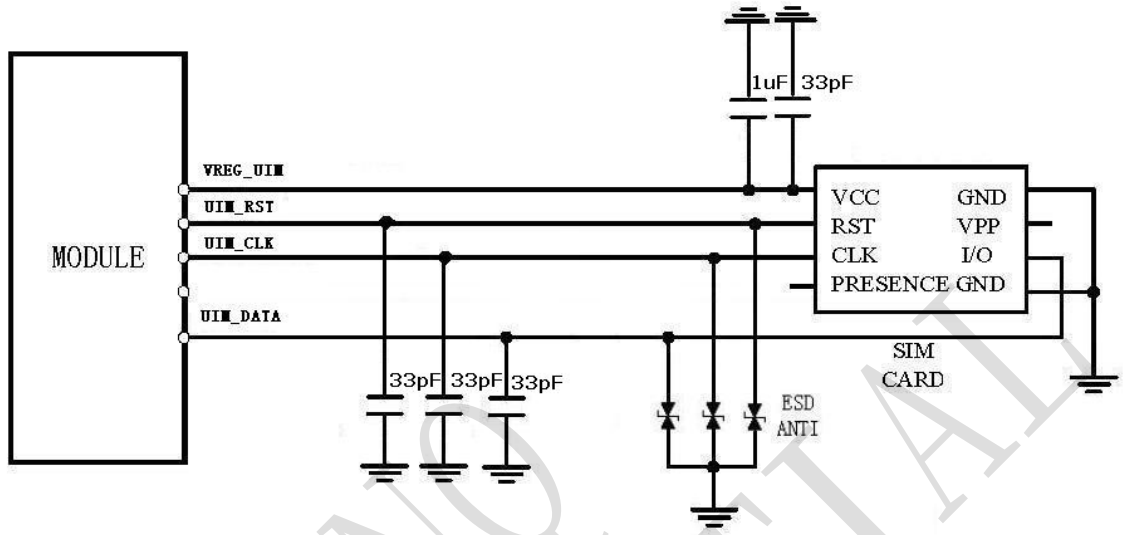


Figure 3-6 USIM Reference circuit

Note: USIM_DATA have added the pull-up resistance in the module design.

3.6 PCM interface

3.6.1 PCM interface definition

L506 provides hardware PCM interface for external codec. L506 PCM interface can be used in short sync master mode only, and only supports 16 bits linear format：

table 3-9 PCM interface definition

Pin No.	Signal name	I/O Type	DC Characteristics (V)		
			Min.	Typ.	Max.
75	PCM_SYNC	PCM synchronizing signal	-0.3	1.8	1.9
74	PCM_DIN	PCM data input	-0.3	1.8	1.9
73	PCM_DOUT	PCM Data output	-0.3	1.8	1.9
76	PCM_CLK	PCM Data clock	-0.3	1.8	1.9

3.6.2 PCM interface application

L506 only support the host mode, PCM_SYNC,PCM_CLK is the output pin， PCM_SYN as the synchronizing output 8kHz sync signal. PCM Data support 8bit or 16bit data.

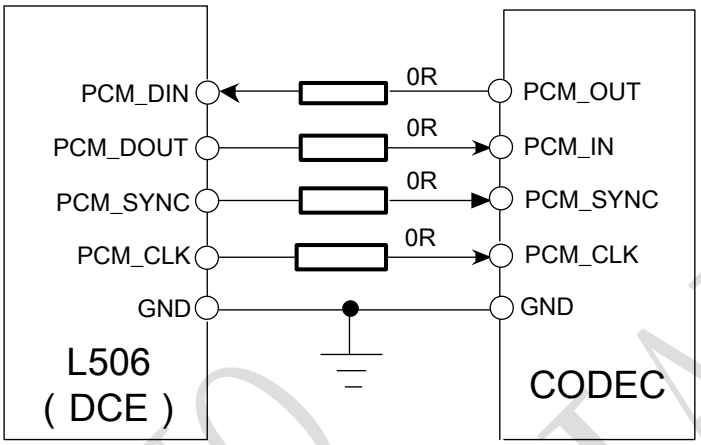


figure 3-7 PCM application circuit (L506 in host mode)

3.7 USB2.0 interface

3.7.1 USB interface pin definition

L506 integrated a USB 2.0 port and low speed mode full speed mode and high speed mode transmission speed between the AP and the host. Table 3-10 is the module USB pin definition

Table 3-10 USB interface pin definition

Pin No.	Signal name	I/O type	DC characteristic (V)		
			Min.	Typ.	Max.
12	USB_DM	USB2.0 date D-	-	-	-
13	USB_DP	USB2.0 data D+	-	-	-

3.7.2 USB Interface application

USB bus is mainly used for data transmission, software upgrading, module testing. Work in the high-speed mode of the USB line, if you need ESD design, ESD protection device must meet the junction capacitance value <5pf, otherwise the larger junction capacitance will cause waveform distortion, the impact of bus communication. Differential impedance of differential data line in 90ohm + 10%.

3.8 UART Interface

3.8.1 Pin description

L506 module provides a flexible 7-wire UART (universal asynchronous serial transmission) interface. UART as a full asynchronous communication interface, Support the standard modem handshake signal control, Comply with the RS - 232 interface protocols. Also support four wire serial bus interface or the 2-wire serial bus interface mode, and the module can be through the UART interface for serial communication with the outside (DET) and the AT command input, etc. L506 module is a DCE (Data Communication Equipment) and client PC is a DTE (Data Terminal Equipment).AT commands are entered and serial communication is performed through UART interface. The pin signal is defined as shown in below table.

table 3-11 UART pin definition

Pin No.	Pin	I/O type	Descriptions
71	UART_TX	DO	UART data transmission
68	UART_RX	DI	UART data receive
69	UART_RI	DO	Ring Indicator.
66	UART_RTS	DO	UART DET request to send
72	UART_DTR	DI	DTE get ready.
67	UART_CTS	DI	UART Clear to Send.
70	UART_DCD	DO	UART Carrier detects.

Note：UART_RI, UART_DTR can be used as two line UART interface for system debugging, See table 3-3 Pin functional description.

3.8.2 electrical characteristics

UART_RI, UART_DTR default status is the system log port, so we recommend that users keep reserved the interface and test points in design. The L506 UART is 1.8V interface. Figure 3-8 and figure 3-9 is application circuit. A level shifter should be used if user's application is equipped with a 3.3V UART interface. The level shifter TXB0108RGYR provided by Texas Instruments is recommended. The reference design of the TXB0108RGYR is in the following figures.

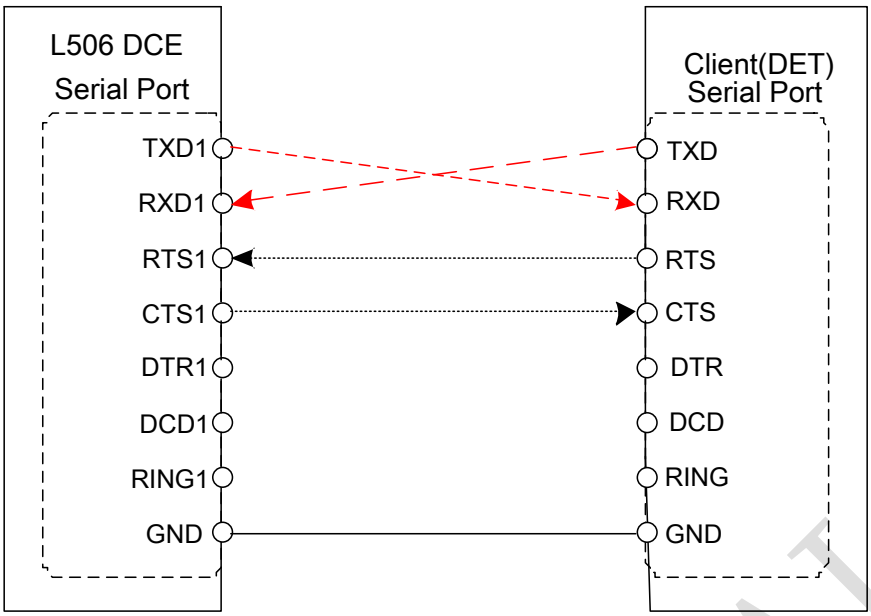


figure 3-8 UART 4 Line connection mode

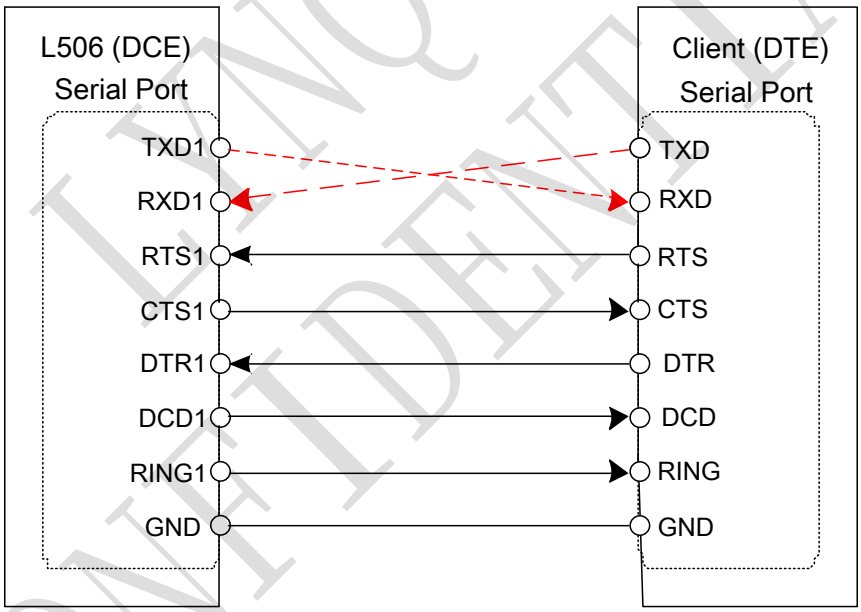


Figure 3-9 UART Full mode

3.9 Keypad interface

3.9.1 pin definition

A typical circuit about the keypad (5*5 keypad matrix) is shown in the following figure.

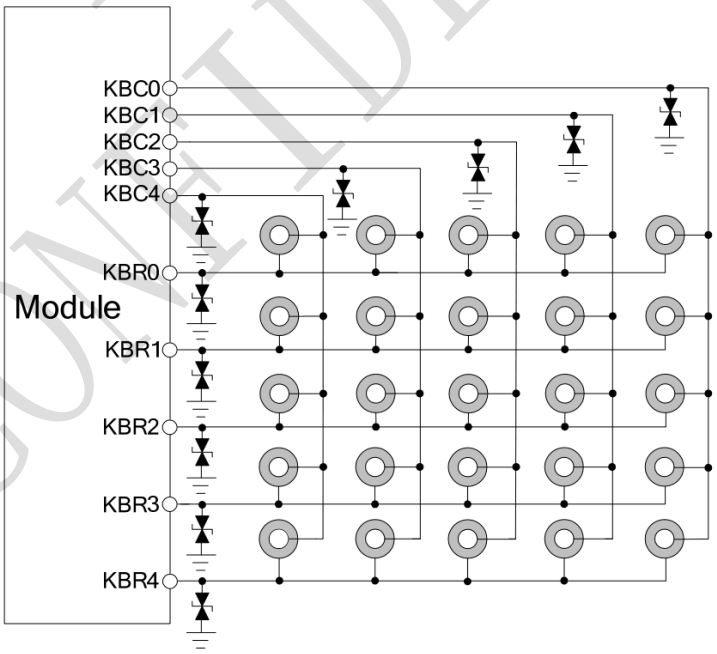
table 3-12 5*5 keypad matrix pin definition

Pin No.	Pin	I/O Type	Descriptions

29	KBR0	DOH	Bit 0 drive to the pad matrix
33	KBR1	DOH	Bit 1 drive to the pad matrix
30	KBR2	DOH	Bit 2 drive to the pad matrix
35	KBR3	DOH	Bit 3 drive to the pad matrix
34	KBR4	DOH	Bit 4 drive to the pad matrix
28	KBC0	DI,PD	Bit 0 for sensing key press on pad matrix
27	KBC1	DI,PD	Bit 1 for sensing key press on pad matrix
31	KBC2	DI,PD	Bit 2 for sensing key press on pad matrix
32	KBC3	DI,PD	Bit 3 for sensing key press on pad matrix
36	KBC4	DI,PD	Bit 4 for sensing key press on pad matrix

3.9.2 Keypad applications

L506 module provides a keypad interface that supports five sense columns, and five keypad rows. The interface generates an interrupt when any key is pressed. Its operation voltage is 1.8V.



fingure 3-10 Keypad Reference Circuit

Note：keypad and can be used as the wakeup pin for AP wake up the module.

3.10 Power on/off and reset interface

3.10.1 Pin definition

L506 can be powered on by pulling PWRKEY pin down to ground. This pin is already pulled up with a 200KΩ resistor to 1.8V in module, so external pull-up resistor is not necessary. Placing a100nF capacitor and an ESD protection diode close to the PWRKEY pin is strongly recommended. Please refer to the following figure for recommended reference circuit.

L506 also have a RESET pin to reset module. This function is used as an emergency reset only when AT command “AT+CPOF” and the PWRKEY pin has no effect. User can pull RESET pin to ground, then module will reset. This pin is already pulled up with a 40KΩ resistor to 1.8V in module, so external pull-up resistor is not necessary. Placing a100nF capacitor and an ESD protection diode close to the RESET pin is strongly recommended. Please refer to the following figure for recommended reference circuit.

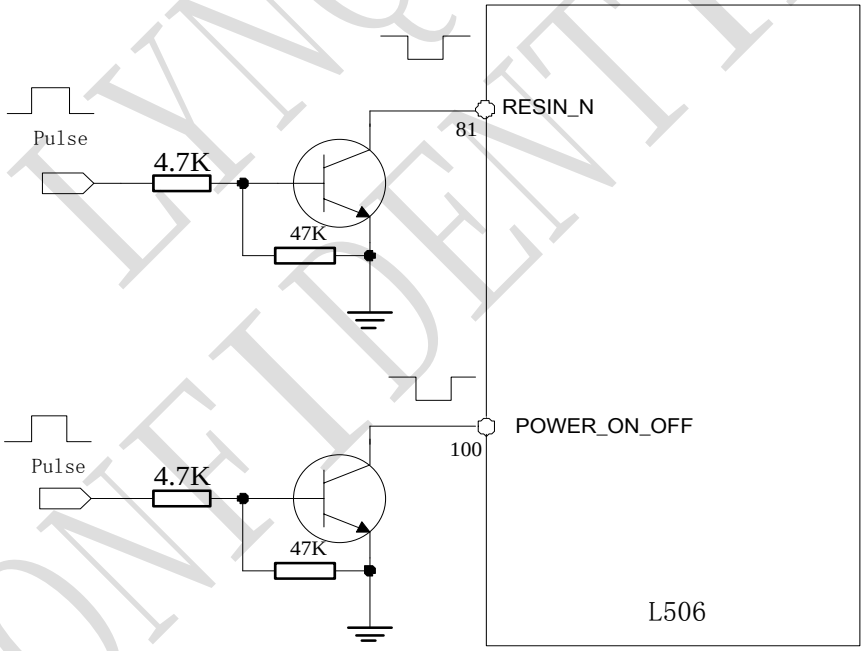


Figure 3-11: Reference power on/off circuit

3.11 Interactive interface

3.11.1 Pin definition

Table 3-14 list the interface is mainly with the application processor interactive interface,

including query, wake up four types, status indication, flight mode interface.

table 3-14 interactive interface

Pin No.	Signal	I/O type	Descriptions
50	GPIO_74	DI	Default: GPIO Optional: Input pin as wake/interrupt signal to module from host.
49	STATUS	DO	AP inquire the module status
54	FLGHTMODE	DI	Pull up to 1.8V made the system enter in flight mode, at this mode will tune off all the wireless function

3.11.2 interface application

L506 provides three shook hands with application processor communication signals. Application processor can query whether the module boot normal work through MDM_POWERON. Through the MDM_READY query module is in sleep mode, and sleep in the module, through AP_WAKEUP _MDM wake module. Similarly, when application processor in the sleep state, the L506 modules can through MDM_WAKEUP_AP wake application processor.

- STATUS：Module sleep instructions, high level indicator to sleep, low level instructions for the awakened state;
- GPIO_74： The host can lower the signal awakens the module，If, low level has maintained, module can't sleep.
- FLGHTMODE：Through the external output high level module into flight mode;

3.12 LED Light interface

3.12.1 Pin define

Table 3-15 LED pin definitions

Pin No.	Net name	I/O type	description
45	Isink	DO	Module state identify control LED port

3.12.2 Led application

The L506 module has 1 pins for controlling the LED display, which can be used as an indicator of network connection status. Different network states are represented by the mode of the flashing

light. This pin is an GPIO，with An external NPN Transistor，External connect VBAT can directly drive LED. Drive current capacity varies according to external NPN model，recommend use DTC143ZEBTL，Drive current biggest can reach 100 mA, below is the reference circuit.

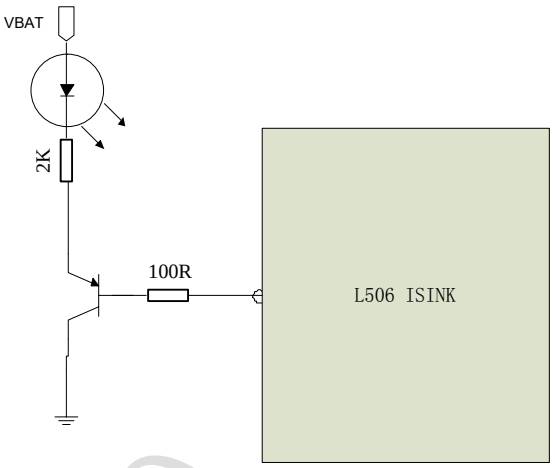


Figure 3-12 Status indicator reference circuit

3.13 SD card interface

3.13.1 Pin descriptions

L506 provides a 4-bit SD/MMC interface with clock rate up to 52MHz. The operation voltage of MMC/SD interface is 2.95V with SD/MMC memory cards up to 2 TB, which is compatible with SDIO Card Specification (version 3.0), Secure Digital (Physical Layer Specification, version 3.0) and Multimedia Card Host Specification MMC (version 4.4)

Table 3-16 SD characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_EXT**	LDO output	-	2.85	-	V
VIH	High-level input voltage	0.625*VDD_EXT	-	VDD_EXT+0.3	V
VIL	Low-level input voltage	-0.3	0	0.25*VDD_EXT	V
VOH	High-level output voltage	2.75*VDD_EXT	2.85	VDD_EXT	V
VOL	Low-level output voltage	0	0	0.125*VDD_EXT	V

SD card I/O load capacity for linear output displacement, concrete can be calculated according to the following chart;

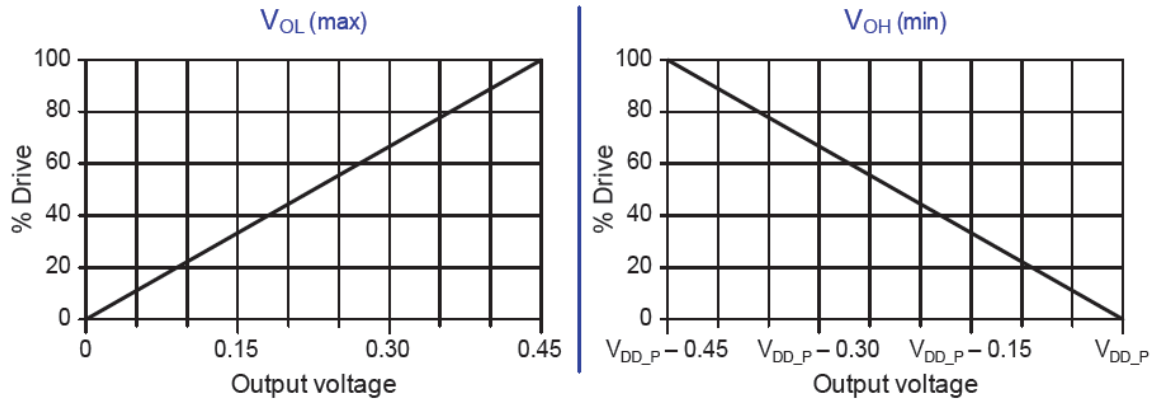


Figure 3-13 VOL/VOH IV curve

3.13.2 SD card interface design guideline

L506 VDD_EXT for external SD card interface of power supply, in the card slot position should add the ESD protection circuit; If you need to support SD hot plug design need to add SD_DET signals. Due to the default hot plug pin of L506 check for low level to identify the card insert status, so you need to choose the detect PIN connected to the ground when SD card is inserted into the SD slot, below is the reference circuit.

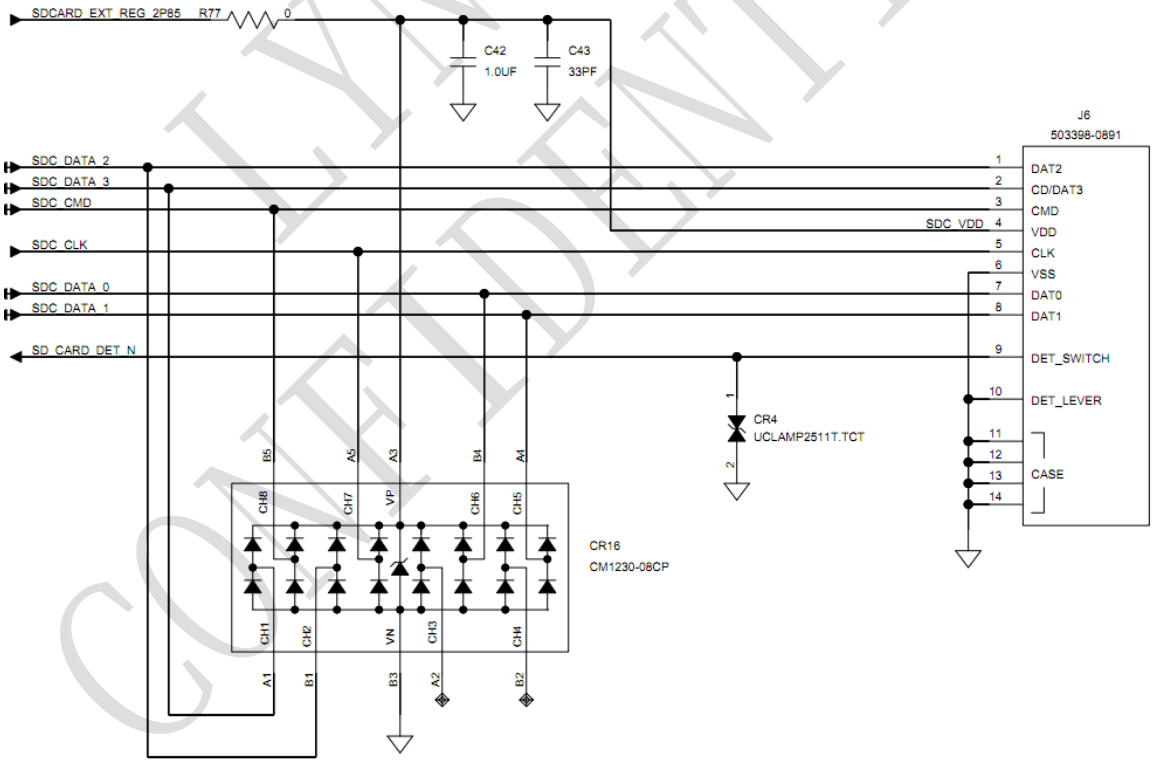


Figure 3-11 SD card recommended circuit

3.13.3 SD card signal PCB line rules

Due to the SD signal is the high-speed digital interface, so it's layout rules should be in accordance with the high speed digital rules.

1.Protect other sensitive signals/circuits from SDC corruption.
2. Protect SDC signals from noisy signals (clocks, SMPS, etc.).
3. 50 Ω nominal, ±10% trace impedance.
4. CLK to DATA/CMD length matching < 1 mm.
5. Total routing length < 50 mm recommended.
6. Spacing to all other signals = 2x line width.6 Bus capacitance < 15 pF.

3.13 I2C interface

3.13.1 I2C pin definition

I2C is used to communicate with peripheral equipment and can be operated as either a transmitter or receiver, depending on the device function. Both SDA and SCL are bidirectional lines connected with I2C interface. Its operation voltage is 1.8V. High speed mode transmission rate can reach 400 KBPS, Because L506 have internal pulled up to the I2C interface, so in your design needn't pull up. Figure 3-15 is the reference design:

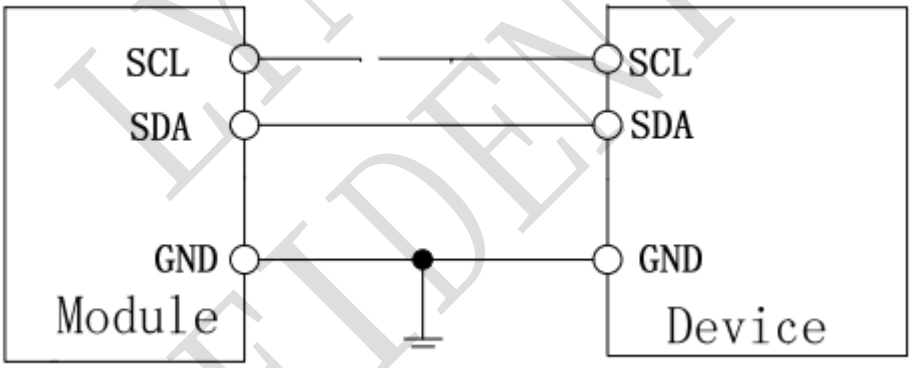


Figure 3-12 I2C reference design

3.14 Antenna interface

3.14.1 RF signal PCB layout guide

L506 provides RF antenna interface. Customer's antenna should be located in the host board and connected to module's antenna pad through micro-strip line or other types of RF trace and the trace impedance must be controlled in 50Ω. we recommends that the total insertion loss between the antenna pad and antenna should meet the following requirements:

- GSM900/GSM850<0.5dB
- DCS1800/PCS1900 <0.9dB
- WCDMA 2100/1900<0.9dB
- WCDMA 900/850<0.5 dB
- TDSCDMA 900/850<0.5dB
- CDMA BC0<0.5dB
- LTE (F<1GHz) <0.5dB
- LTE (1GHz<F<2GHz) <0.9dB
- LTE (2GHz<F) <1.2dB

To facilitate the antenna tuning and certification test, a RF connector and an antenna matching circuit should be added. The following figure is the recommended circuit.

The antenna feed point is defined as shown in table 3-17：

table 3-1 antenna pin definition

Pin No.	Signal	I/O Typ.	Description
82	MAIN_ANT	AI/AO	Module main antenna
59	AUX_ANT	AI	LTE diversity antenna feed point
79	GNSS_ANT	AI	GNSS antenna feeder connector

3.14.2 applications

For convenience of antenna tuning and certification test, should increase RF connectors and the antenna matching circuit, below is a recommended circuit:

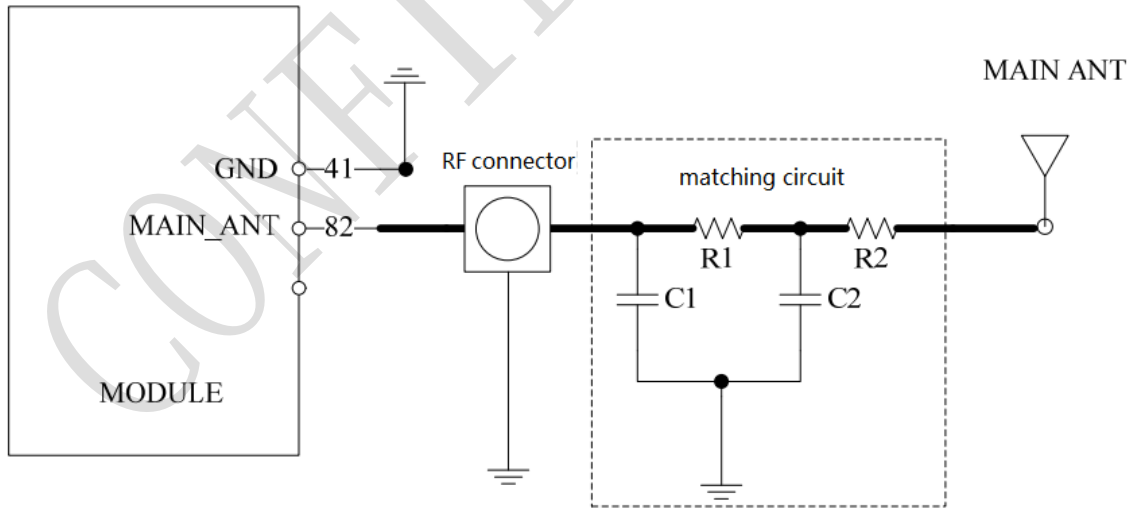


Figure 3-13 Main antenna matching circuit diagram（**MAIN_ANT**）

In this figure, the components R1, C1, C2 and R2 is used for antenna matching, the value of components can only be got after the antenna tuning, usually, they are provided by antenna vendor. By default, the R1, R2 are 0 Ohm resistors, and the C1, C2 are reserved for tuning.

The RF test connector in the figure is used for the conducted RF performance test, and should be placed as close as to the module's antenna pin. The traces impedance between components must be controlled in 50ohm.

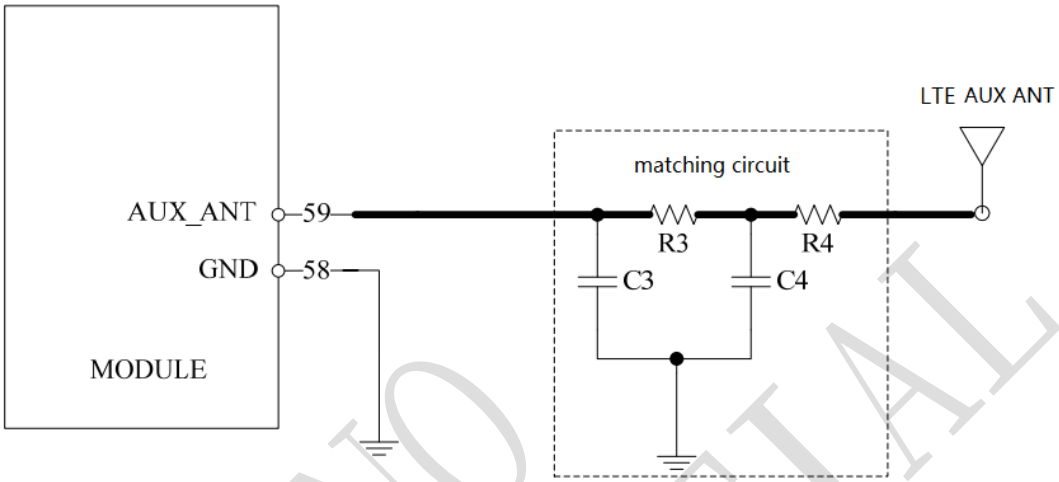


Figure 3-14 LTE Diversity antenna matching circuit diagram（**AUX_ANT**）

Note：LTE diversity antenna recommend leaving. Because there are many high frequencies of TDD LTE design, such as band38 band40 and Band41. Due to the high insertion loss RF line, if there is no diversity antenna, receiving sensitivity of the spectrum in the certification will be a risk.

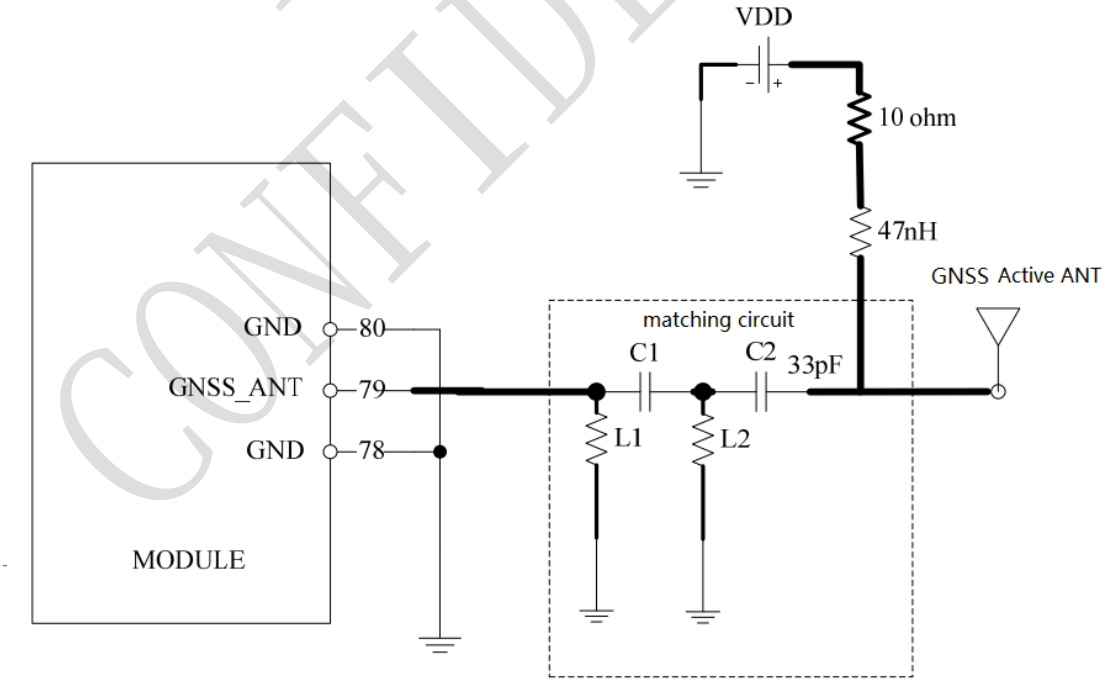


Figure 3-18 GNSS active antenna matching circuit diagram（GNSS_ANT）

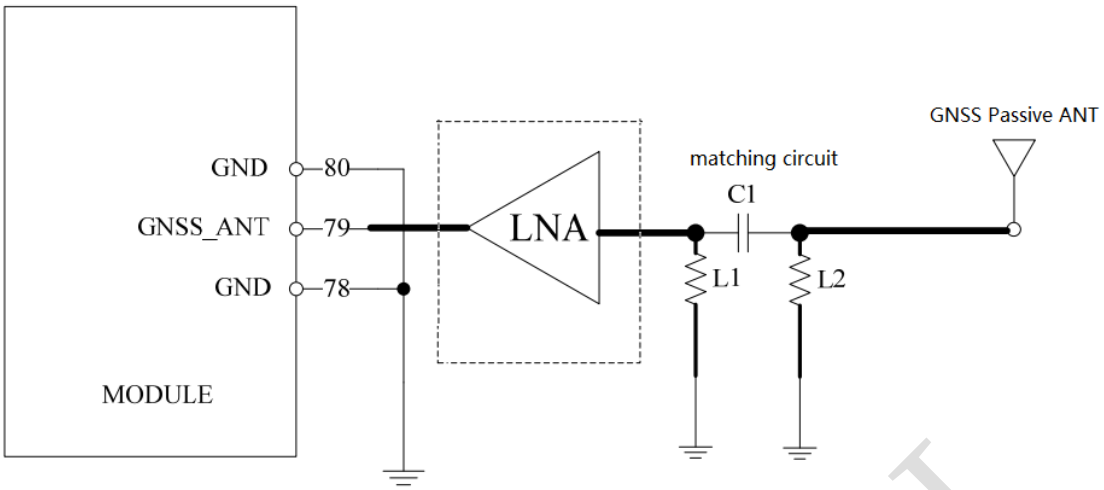


Figure 3-19 GNSS passive antenna matching circuit diagram（GNSS_ANT）

In above figures, the components C1 and L1, L2 are used for antenna matching, the values of the components can only be obtained after the antenna tuning usually, and they are provided by antenna vendor.C2 in Figure 3-19 is used for DC isolation. In active antenna circuit, users must use an external LDO/DCDC to provide VDD voltage whose value should be taken according active antenna characteristic, and VDD can be shut down to avoid consuming additional current when not being used. GNSS can be used by NMEA port. User can select NMEA as output through UART or USB. NMEA sentences are automatic and no command is provided. NMEA sentences include GSV, GGA, RMC, GSA, and VTG. Before using GNSS, user should configure L506 in proper operating mode by AT command.

Please refer to related document for details. L506 can also get position location information through AT directly.

In the diagram above, component C1, L1 and L2 for antenna match, the element's value depends on the antenna after debugging. In figure 3-18, C2 for dc isolation. In the active antenna circuit, the user must use an external "/ DCDC VDD voltage, its value should be according to the properties of the active antenna, VDD can close to avoid without additional current consumption when using GNSS. In figure 3-19, the user can increase a external LNA gain to get better.

L506 merges GNSS (GPS/GLONASS) satellite and network information to provide a high-availability solution that offers industry-leading accuracy and performance. This solution performs well, even in very challenging environmental conditions where conventional GNSS receivers fail, and provides a platform to enable wireless operators to address both location-based services and emergency mandates.

Tracking sensitivity -159 dBm（GPS） -158 dBm（GLONASS）
AcquisitionSensitivity -148dBm
Cold-start sensitivity -142 dBm
C/N0 = S - (-170) S= Input Signal Intensity
Accuracy (Open Sky) 2.5m (CEP50)
TTFF (Open Sky) Hot start <1s Cold start 35s

Receiver Type 16-channel, C/A Code
GPS L1 Frequency (1575.42±1.023MHz),
GLONASS: 1597.5~1605.8 MHz
Update rate Default 1 Hz
GNSS data format NMEA-0183
GNSS Current consumption (WCDMA/GSM Sleep mode) 100mA (Total supply current)

Antenna Layout guideline

In layout design, antenna RF transmission line must ensure the characteristic impedance = 50 ohm. The characteristic impedance depend on substrate board, line width and the distance from the ground plane. As shown in figure 3-20 is the layout of antenna feed point of reference for clearance area.

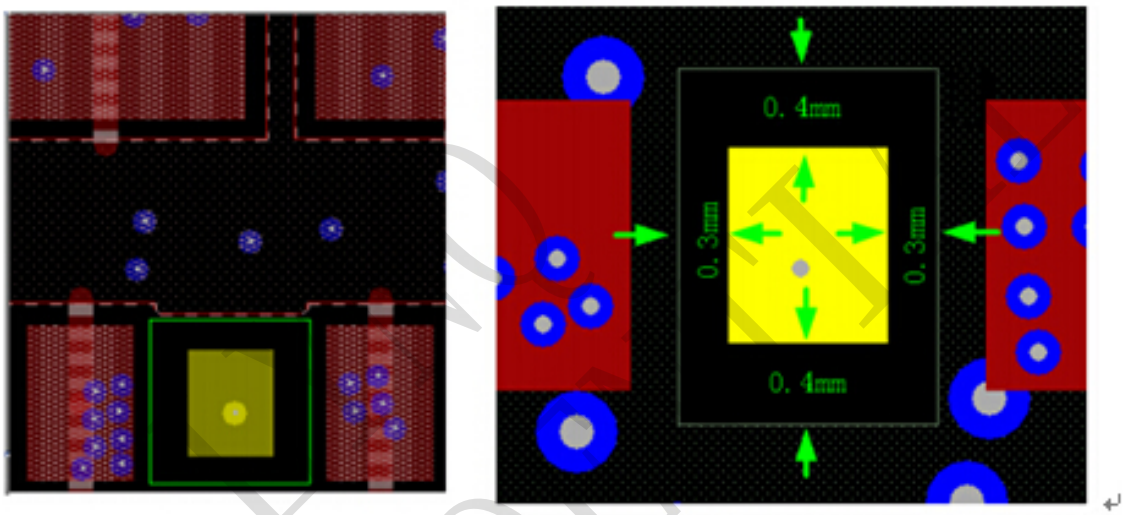


Figure 3-20 antenna feed point

4 Product characteristics

4.1 Power characteristics

4.1.1 power supply

This product is a DC input voltage range of 3.4 V to 4.2 V, the typical value of 3.8 V, as shown in table 4-1.

Table 4-1 Input DC voltage

Parameter	Min.	Typ.	Max.
Input Vol.	3.4V	3.8V	4.2V

4.1.2 Power on/off Sequence

Boot process is divided into two cases: first on electricity and system operation process to enable the module. Two cases of the same process, as shown in figure 4-1.

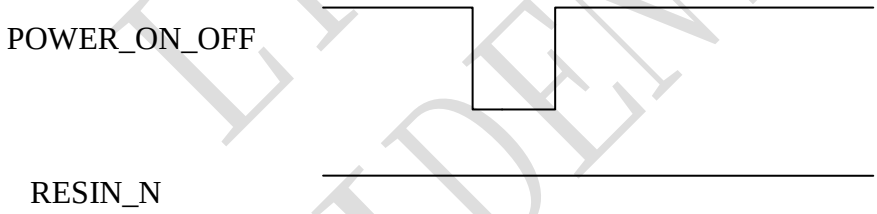


Figure 4-1 Power on sequence

As shown, application processor to control POWER_ON_OFF form under pulse, pulse width should be in 8 seconds. Before the falling edge of the POWER_ON_OFF, module does not work, in a state of power lost. When the module detects POWER_ON_OFF began after the falling edge of electricity on boot, After initialization start USB enumeration, application processor side a USB device file. Shutdown process occurs in the whole system is in the process of the operation and close the module. The shutdown process as follows:

(1). If the PPP connection has been established, please disconnect.

(2). The application processor used AT + COPS = 2 command log off from the network;

(3). Application processor used AT + CPOF command notification module to turn it off.

In the process of the above, POWER_ON_OFF and RESIN_N signals always maintained high level.

When the module is received after the AT + CPOF command, will be cleared and save the module of data operation, and control module. Application processor without waiting for the outcome of the

AT + CPOF command code, just wait for the USB serial port devices.

4.1.3 Reset Process

When application processor need to reset the module, the control under the RESIN_N reset signal pulse, pulse width need to be larger than 2ms, recommended width 200 Ms. POWER_ON_OFF keep for high level signals. Module reset process as shown in figure 4-2.

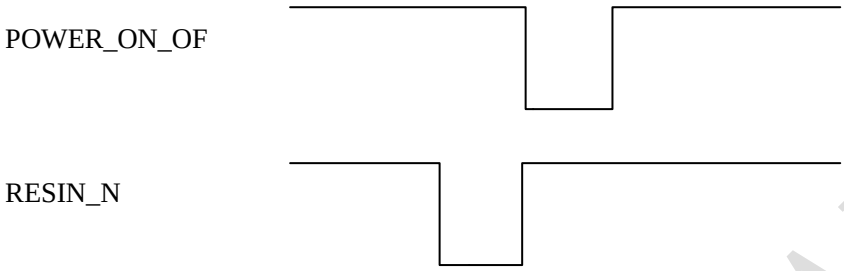


Figure 4-2 The illustration of module to reset

When RESIN_N pulled up, POWER_ON_OFF signal to generate a pulse, the pulse width requirements like the boot process.

5 Design guideline

This chapter provides a general design of the products instruction, the user can refer to design guidance for design, make products to achieve better performance.

5.1 General design rules and requirements

Users in the design of this product is peripheral circuit, the first to ensure the external power supply circuit can provide enough power supply capacity, And the requirements for high speed signal lines USB control 90 ohm + / - 10% difference impedance. For general signal interface, require the user to us in strict accordance with the requirements of design, in line with the interface signal level matching, in case the level of damage to the module. This product its own radio frequency index is good, customers need to design in accordance with the requirements the mainboard side antenna circuit and corresponding impedance control, otherwise it will affect the whole RF index.

5.2 Reference circuit

Request system board VPH_PWR side power supply ability of power supply to achieve more than 2 A, meet the demand of modules, peak current, and the system side the power of the average current will reach more than 0.9 A. System board side power supply cord shall ensure enough line width, and wants to form a good return with the ground plane, moreover should increase in the power supply circuit design the method of micro level energy storage capacitor, guarantee the instantaneous power supply capacity, and the power supply ripple control within the 100 mv, the specific function of each functional module can be found in the corresponding description, overall reference circuit design 5-1.

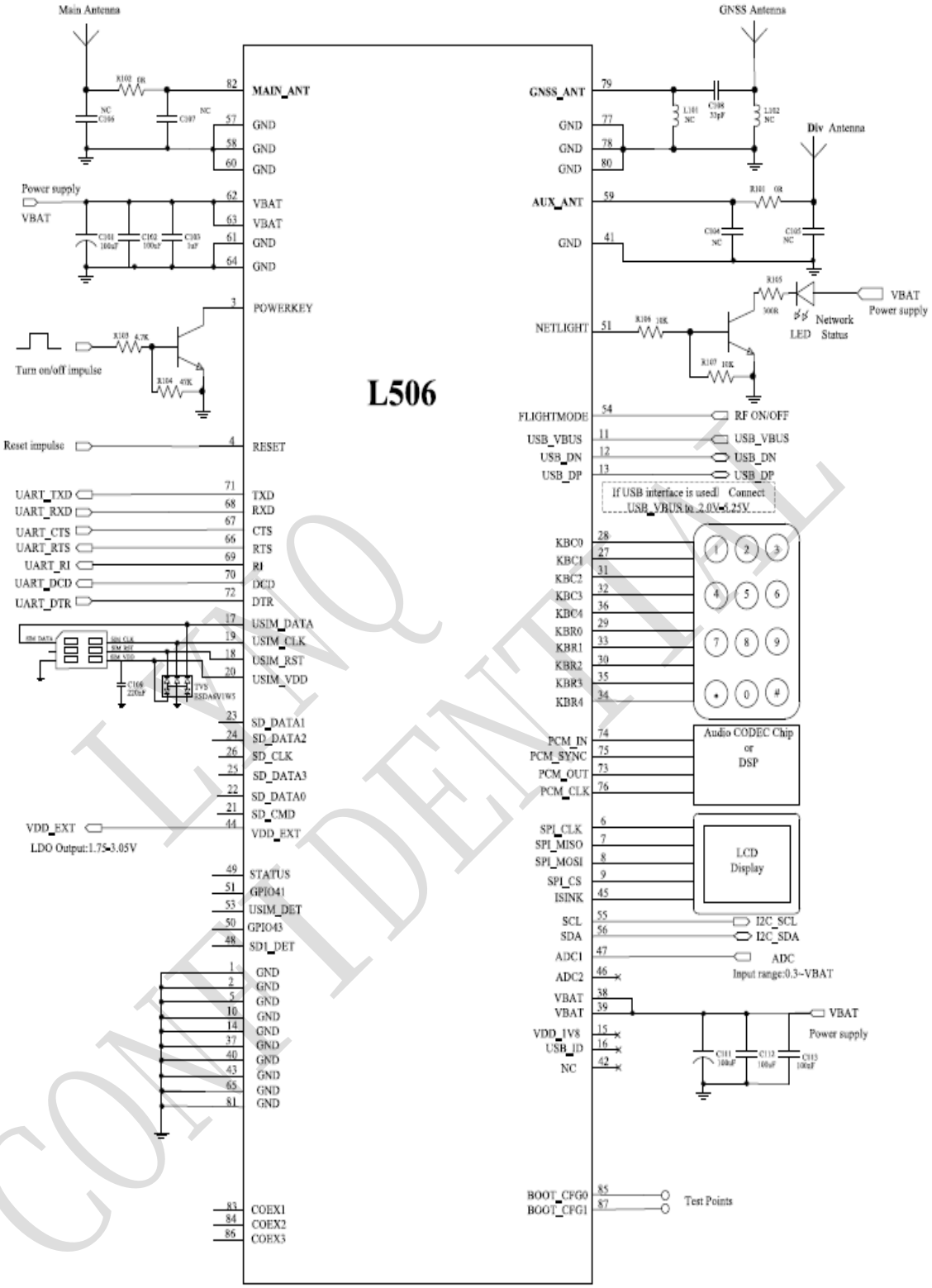


Figure 5-1 L506 reference circuit

5.3 RF part design guideline

5.3.1 Early antenna design considerations

- Pre project evaluation

The selection of the antenna position must first ensure that the antenna and the base station are kept in the horizontal direction, this produces the highest efficiency; Secondly, try to avoid placing the switch in the power supply or data line, chip and other devices or chips that produce electromagnetic interference. At the same time, the position of the hand can be avoided, so as to prevent the human body to produce attenuation; But also to reduce the radiation and the structure of the realization of the need to take into account. So, At the beginning of the design need to structure, ID, circuit, antenna engineers together to evaluate the layout.

- Antenna matching circuit

If the module's radio frequency port and the antenna interface need to be transferred, the main board circuit design, The design of microstrip line or strip line between the module RF test base and the antenna interface between the microstrip line or the strip line by characteristic impedance 50 ohm, at the same time, reserved double L type matching circuit; If the antenna's RF connector can be directly stuck in the module's RF test base, can save the module of the RF port and the antenna interface between the transfer.

5.4 EMC and ESD design advice

Users should take full account of the EMC problem caused by signal integrity and power integrity in the design of the whole machine, In the module of the peripheral circuit layout, for power and signal lines, etc., to maintain the spacing of 2 times line width. Can effectively reduce the coupling between the signal, so that the signal has a clean, the return path. When the peripheral power supply circuit is designed, the decoupling capacitor should be placed close to the module power supply pin, High frequency high speed circuit and sensitive circuit should be far from the edge of PCB, and the layout of the layout as far as possible to reduce the interference between each other, and the sensitive signal is protected. The circuit or device that may interfere with the operation of the system board is designed.

This product is embedded in the system board side, design, need to pay attention to the ESD protection, the key input and output signal interface, such as (U) SIM card interface need to be placed close to the protection of ESD devices. In addition to the

motherboard side, the user is required to design the structure and PCB layout, ensure that the metal shield is fully grounded, and set up an unobstructed discharge passage for the electrostatic discharge.

5.5 PCB Recommended land pattern

We recommend that users in the design of main board PCB DEF，In the middle of the 12 geothermal solder design according to size in figure 5-3. Recommended at 87 of peripheral signal pads to the module with a length of 1.0 mm.

Recommended PCB pads as shown in figure5-2:

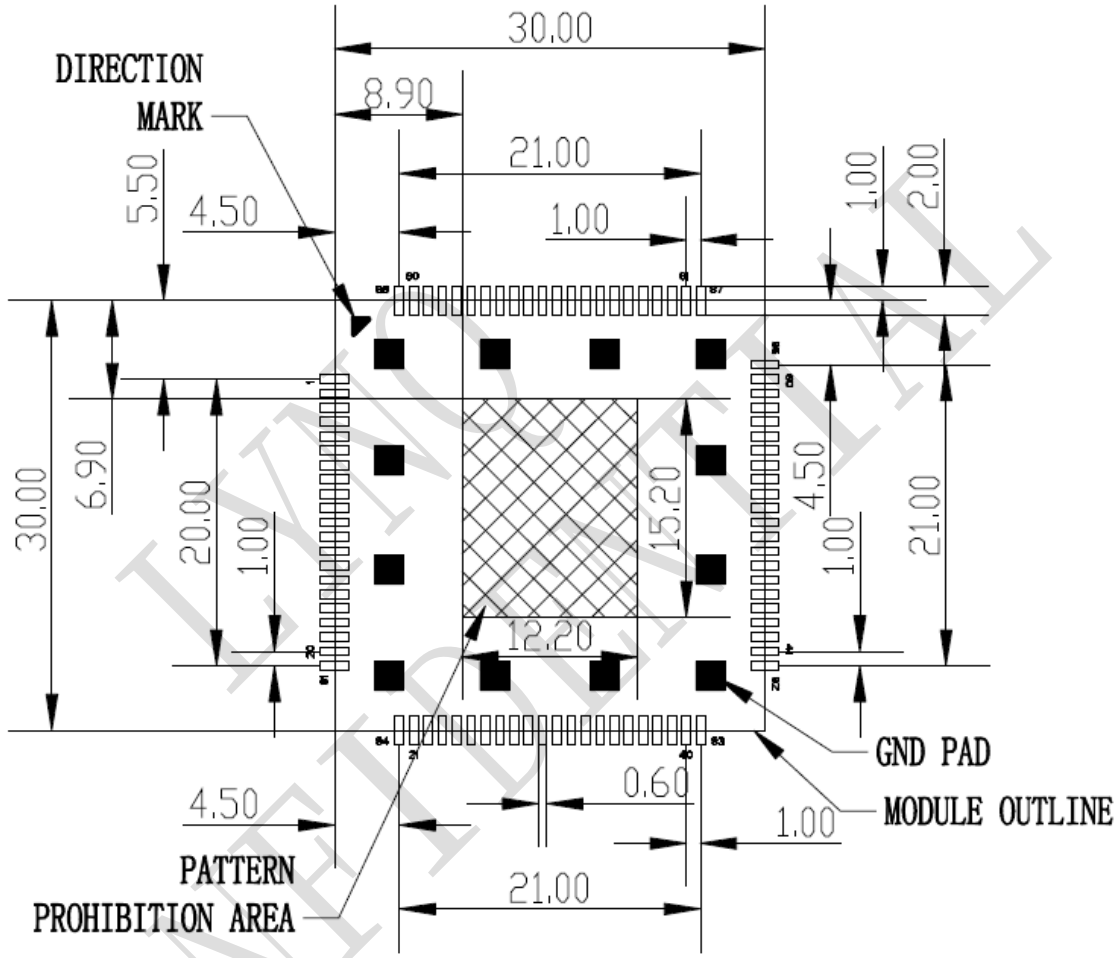


Figure 5-2 RECOMMENDED LAND PATTERN (Unit: mm) (detail A)

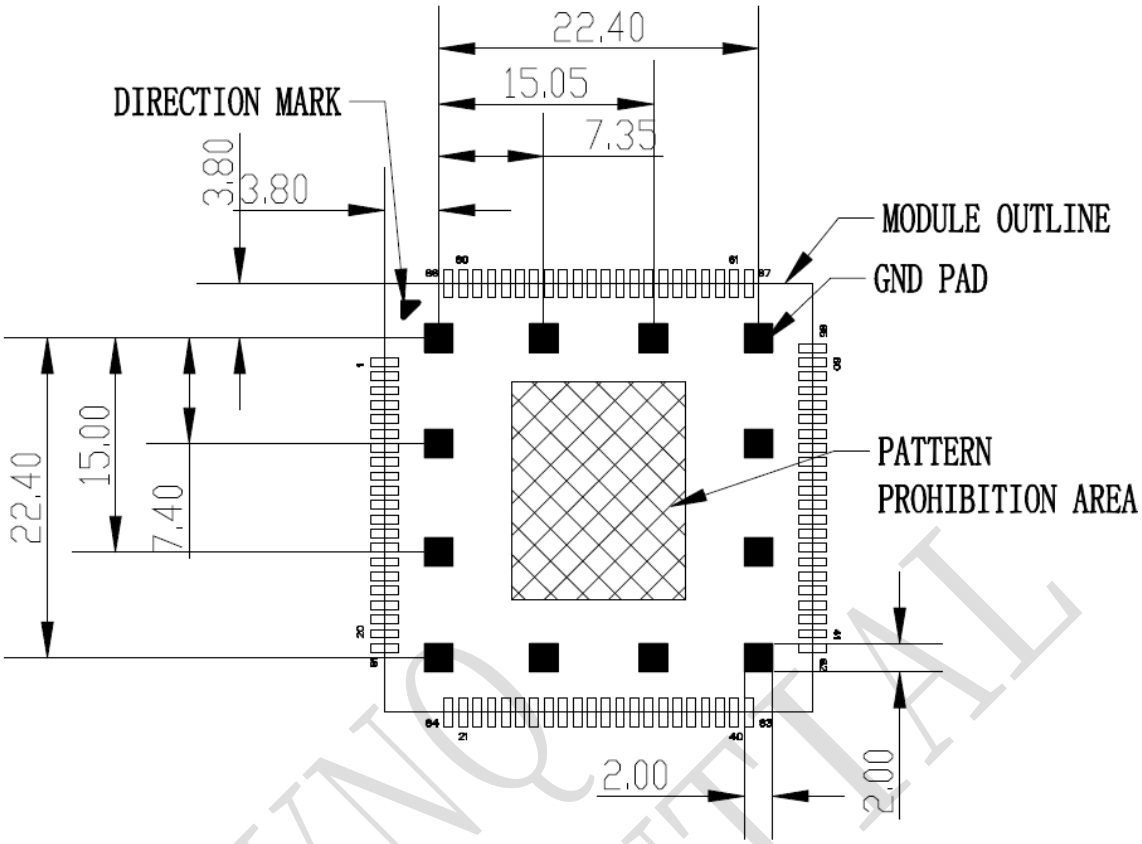


Figure 5-1 RECOMMENDED LAND PATTERN (Unit: mm) (detail B)

5.6 Operating Temperature

The operating temperature of L506 is listed in the following table.

Table 32: Operating temperature

Parameter	Min.	Typ.	Max.	Unit
Normal operation temperature	-30	25	80	℃
Extended operation temperature*	-40	25	85	℃
Storage temperature	-45	25	90	℃

Note: Module is able to make and receive voice calls, data calls, SMS and make GPRS/WCDMA/HSPA+/LTE traffic in -40℃ ~ +85℃. Temperatures outside of the range -30℃ ~ +80℃ might slightly deviate from ETSI specifications.

5.7 Products recommended upgrade

L506 default through the USB firmware updates, so products to facilitate the software update, when the design proposal to set aside the USB test points or interface to facilitate subsequent product of the firmware upgrade.

6 Manufacturers

6.1 Steel mesh design

- At the bottom of the module pad thermal, can be reduced by way of steel mesh openings, reduce the risk of short circuit between the thermal and the module of the module Pin, have certain effect;
- Module pad thermal welded steel mesh openings are recommended for reference. Figure 6-1 is recommended for steel mesh and size.

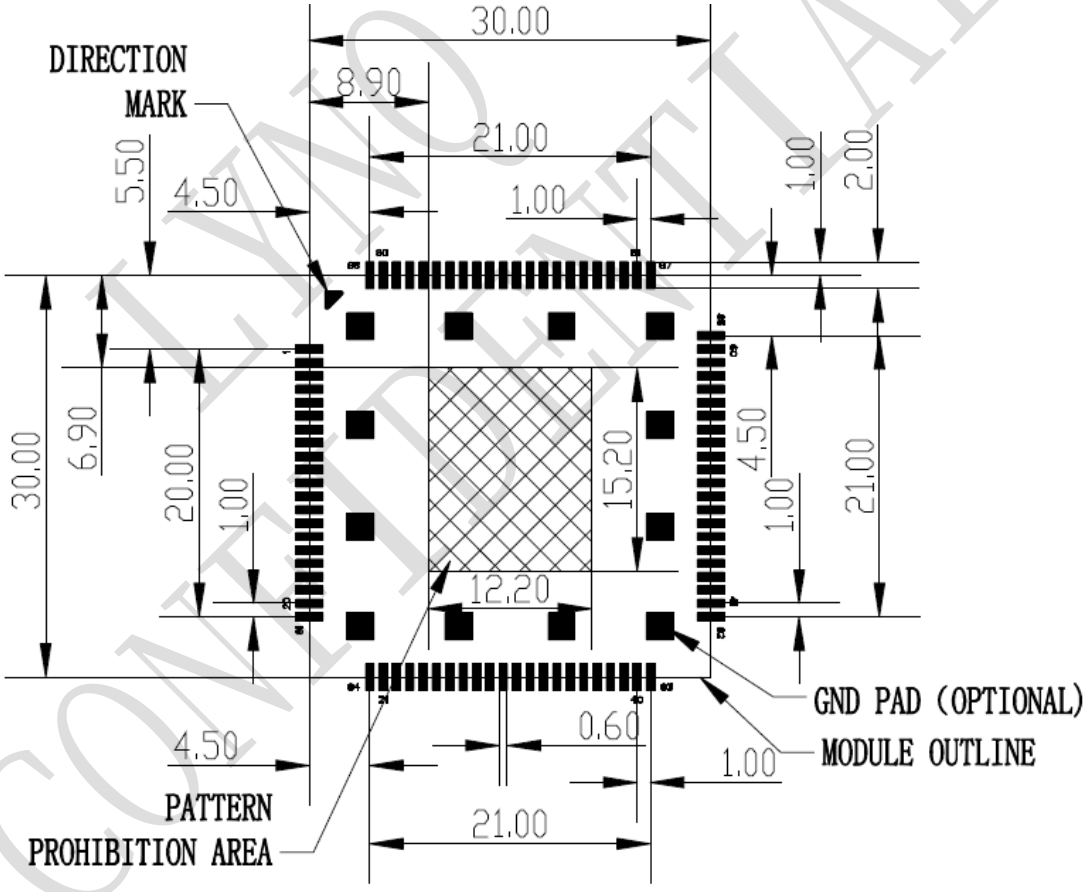


Figure 6-11 Steel mesh (unit mm)(detail A)

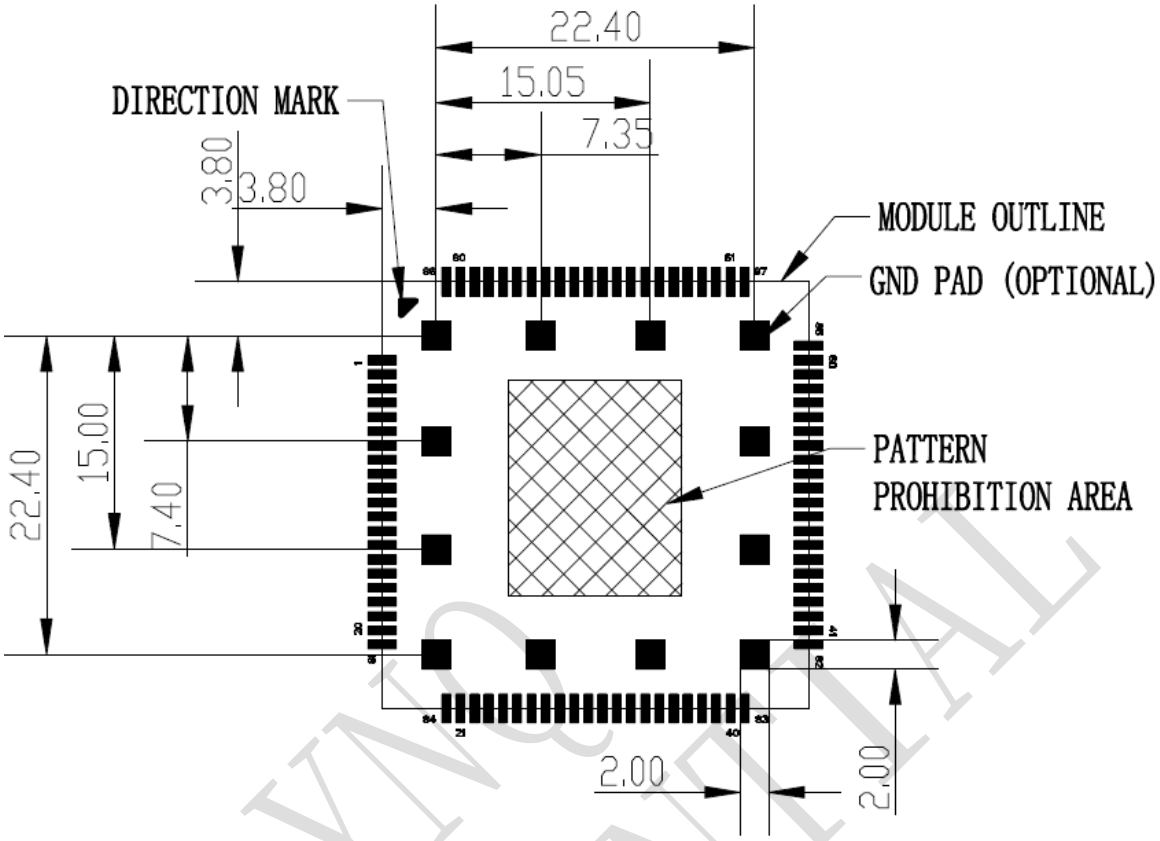


Figure 6-2 Steel mesh (unit mm) (detail B)

6.2 Temperature curve

The temperature curve of the welding quality and material status influence, please pay special attention. Temperature rise speed should not be too fast, from room temperature to 150, the temperature rise rate is less than 3s. At the same time in more than 217 degrees, please try to keep time no more than 70 seconds, at intermediate values of 55 seconds is appropriate. The thermal shock strength is too general will lead to part of the device failure, resulting in a decline in yield and maintenance difficulty. And please control the maximum temperature of no more than 245 degrees, partial material, such as crystal at high temperature easy to occur the package rupture, cause unable to play the problem, and then affect the function of the product, The temperature can be set using the curve shown in table 6-1.

Table 6-1 Temperature curve

Lead-free process temperature curve		
Stage	Temperature	time
Preheat	Temperature rise from room temperature to 150	rate of temperature rising <3 / ℃ s
keep warm	150℃~200℃	40~110 s

Welding	< 217℃	40~70 s
	< 230℃	15~45 s
	Peak temperature	MAX：245℃
		MIN：230℃

PWI= 74%	Maximum temperature ascending slope		Maximum temperature descending slope		Preheat time 150200C		Time of the reflow temperature or above271C		Upper limit		Total time	/230C
Module edge point	1.3	-34%	-1.9	55%	49.6	-72%	57.4	16%	238.7	16%	29.5	-3%
Module bottom	1.3	-35%	-1.8	60%	49.1	-74%	56.2	8%	238.1	8%	28.2	-12%
Chip	1.4	-29%	-2.1	46%	52.7	-64%	63.6	57%	242.5	66%	39.6	64%
Temperature difference	0.1		0.3		3.6		7.4		4.3		11.4	

Process limit

Butter of antimony: Define Your Own Spec

Statistic name	Lower limit	Upper limit	Unit
Maximum temperature ascending slope (target: 2.0) (Time distance = 20 seconds)	0.0	3.0	Degree per second
Maximum temperature descending slope (Time distance = 20 seconds)	-5.0	-1.0	Degree per second
Preheat time 150200C	40	110	Seconds
Time of the reflow temperature or above271C	40	70	Seconds
Maximum temperature	230	245	Degree centigrade
Time of the temperature above 230C	15	45	Seconds

Figure 6-3 The reference temperature curve