

DP1276 – C169/C433/C868/C915

Low Power Long Range Transceiver Module

Combine Small Form Factor with High Performance

Variants for 169 MHz, 433 MHz, 868 MHz and 915 MHz

GENERAL DESCRIPTION

The DP1276 includes the LoRa™ long range modem that provides ultra-long range spread spectrum communication and high interference immunity whilst minimizing current consumption.

Using Semtech's patented LoRa™ modulation technique DP1276 can achieve sensitivity of over -137 dBm. The high sensitivity combined with the integrated +20 dBm power amplifier yields industry leading link budget making it optimal for any application requiring range or robustness. LoRa™ also provides significant advantages in blocking and selectivity over conventional modulation techniques. Solving the design compromise between range, interference immunity and energy consumption.

These devices also support high performance (G)FSK modes for Wireless M-Bus, IEEE802.15.4g and similar compatibility modes. The DP1276 deliver exceptional phase noise, selectivity, receiver linearity and IIP3 for significantly lower current consumption than competing devices.

APPLICATIONS

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control
- Long range Irrigation Systems

KEY PRODUCT FEATURES

- LoRa™ Modem
- 168 dB maximum link budget
- +20 dBm - 100 mW constant RF output vs. V supply
- +14 dBm high efficiency PA
- Programmable bit rate up to 300 kbps
- High sensitivity: down to -148 dBm
- Bullet-proof front end: IIP3 = -12.5 dBm
- Excellent blocking immunity
- Low RX current of 10.3 mA, 200 nA register retention
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK, LoRa™ and OOK modulation
- Built-in bit synchronizer for clock recovery
- Preamble detection
- 127 dB Dynamic Range RSSI
- Automatic RF Sense and CAD with ultra-fast AFC
- Packet engine up to 256 bytes with CRC
- Built-in temperature sensor and low battery indicator

DEVICE OPTIONS

Part	Frequency band	Pin Package
DP1276C169	138 -169 MHz	Board
DP1276C433	433 - 434 MHz	Board
DP1276C868	862 - 920 MHz	Board

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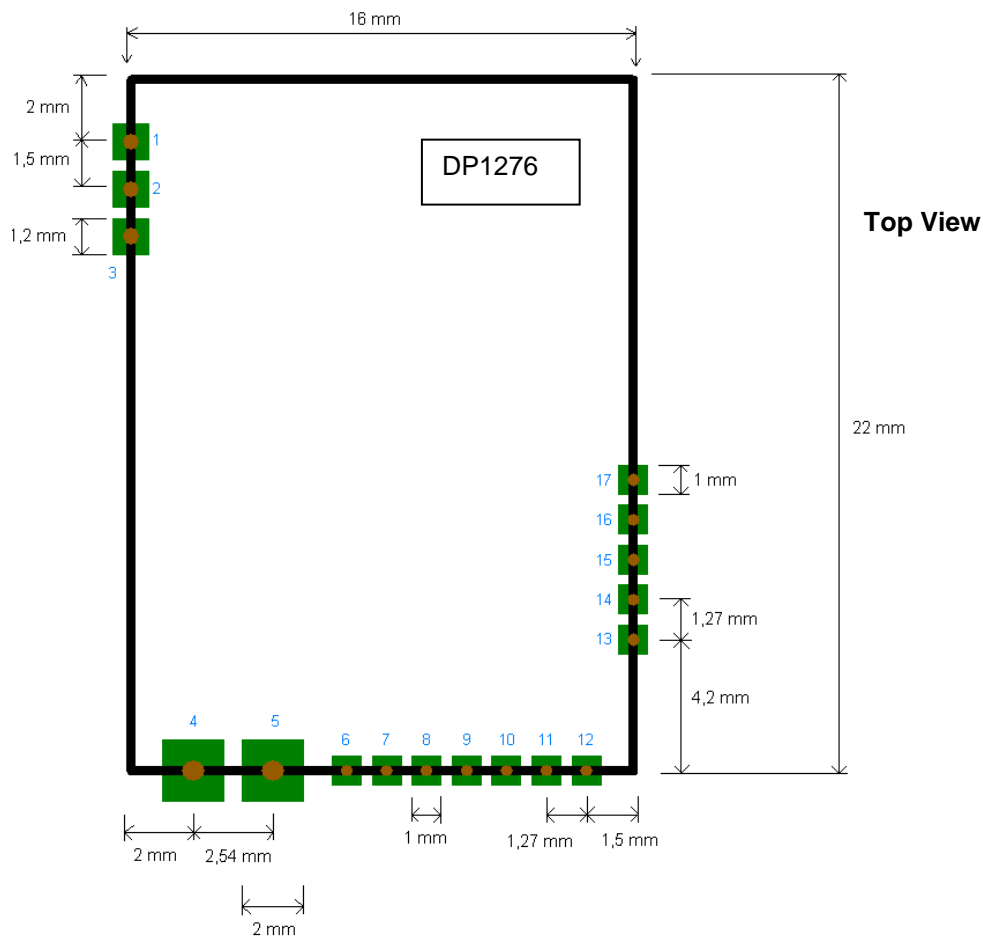
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1. PIN DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	GND		Ground.
2	RFIO	IN/OUT	RF input / output
3	GND		Ground.
4	VDD		Supply voltage.
5	GND		Ground.
6	RESET	IN	Reset trigger input.
7	DIO0	IN/OUT	Digital I/O, software configured.
8	DIO1/DCLK	IN/OUT	Digital I/O, software configured.
9	DIO2/DATA	IN/OUT	Digital I/O, software configured.
10	DIO3	IN/OUT	Digital I/O, software configured.
11	DIO4	IN/OUT	Digital I/O, software configured.
12	DIO5	IN/OUT	Digital I/O, software configured.
13	SCK	IN	SPI Clock input.
14	MISO	Out	SPI Data output.
15	MOSI	IN	SPI Data input.
16	NSS	IN	SPI Chip select input.
17	SWXOVDD	IN	C169 VDD for TCXO and Switch depower in Sleep mode / C433, C868, C915 VDD RF-Switch depower in Sleep mode.

Table 1

2. ELECTRICAL CHARACTERISTICS

2.1. ABSOLUT MAXIMUM RATINGS

Description	Min	Max	Unit
Supply voltage	0.5	3.9	V
Operating temperature	-55	+115	°C
RF Input Level	-	+10	dBm
Load capacitance on digital ports	-	25	pF

Table 2

2.2. OPERATING RANGE

Description	Min	Max	Unit
Supply voltage	1.8	3.7	V
Operating temperature	-40	+85	°C
Load capacitance on digital ports	-	25	pF
RF Input Level	-	+10	dBm
Soldering temperature (max 15 sec)	-	260	°C

Table 3



CAUTION: ESD sensitive device.

Precaution should be taken when handling the device in order to prevent permanent damage



Life Support Policy and Use in Safety Critical Applications

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WIRELESS PRODUCTS

3. SPECIFICATIONS

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VDD=3.3 V, temperature = 25 °C, FXOSC = 32 MHz, F_{RF} = 169/434 MHz (see specific indication), P_{out} = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified. Shared Rx and Tx path matching.

Note: Specification corresponds to the performance in Band 1, Band 2 and Band 3, as described in section 3.2

3.1. POWER CONSUMPTION SPECIFICATION

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in Sleep mode		-	1	1.5	µA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.5	-	µA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.6	1.8	mA
IDDFS	Supply current in Synthesizer mode	FSRx	-	5.8	-	mA
IDDR	Supply current in Receive mode	LnaBoost Off, Bands1&2 LnaBoost On, Bands1&2	- -	10.8 12	- -	mA
IDDT	Supply current in Transmit mode with impedance matching	RFOP = +20 dBm, on PA_BOOST RFOP = +17 dBm, on PA_BOOST	- -	120 87	- -	mA

Table 4

3.2. FREQUENCY SYNTHESIZER SPECIFICATION

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range	Band 1 Band 2 Band 3 Programmable	137 410 862	- - -	175 525 920	MHz
FXOSC	Crystal oscillator frequency		-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time		-	250	-	µs
TS_FS	Frequency synthesizer wake-up time to PLLock signal	From Standby mode	-	60	-	µs
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target frequency	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 50 50 50	- - - - - - -	µs
FSTEP	Frequency synthesizer step		-	61.0	-	Hz
FRC	RC Oscillator frequency		-	62.5	-	kHz
BRF	Bit rate, FSK	Programmable values (1)	1.2	-	300	kbps
BRA	Bit Rate Accuracy	ABS(wanted BR - available BR)	-	-	250	ppm
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps
BR_L	Bit rate, LoRa™ Mode	From SF6, BW=500kHz to SF12, BW=7.8kHz	0.018	-	37.5	kbps
FDA	Frequency deviation, FSK (1)	Programmable FDA + BRF/2 ≤ 250 kHz	0.6	-	200	kHz

Table 5

Note: For Maximum Bit rate the maximum modulation index is 0.5.

WIRELESS PRODUCTS

3.3. FSK/OOK MODE RECEIVER SPECIFICATION

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in RegRxBw, receiving a PN15 sequence. Sensitivities are reported for a 0.1% BER (with Bit Synchronizer enabled), unless otherwise specified. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the receiver sensitivity level.

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F_LF	Direct tie of RFI and RFO pins, shared Rx, Tx paths FSK sensitivity, highest LNA gain. Bands 1&2	FDA = 5 kHz, BR = 1.2 kb/s	-	-121	-	dBm
		FDA = 5 kHz, BR = 4.8 kb/s	-	-117	-	dBm
		FDA = 40 kHz, BR = 38.4 kb/s*	-	-107	-	dBm
		FDA = 20 kHz, BR = 38.4 kb/s**	-	-108	-	dBm
		FDA = 62.5 kHz, BR = 250 kb/s***	-	-95	-	dBm
	Split RF paths, LnaBoost is turned on, the RF switch insertion loss is not accounted for. Bands 1&2	FDA = 5 kHz, BR = 1.2 kb/s	-	-123	-	dBm
		FDA = 5 kHz, BR = 4.8 kb/s	-	-119	-	dBm
		FDA = 40 kHz, BR = 38.4 kb/s*	-	-109	-	dBm
		FDA = 20 kHz, BR = 38.4 kb/s**	-	-110	-	dBm
		FDA = 62.5 kHz, BR = 250 kb/s***	-	-97	-	dBm
RFS_F_HF	Direct tie of RFI and RFO pins, shared Rx, Tx paths FSK sensitivity, highest LNA gain. Band 3 /868/915	FDA = 5 kHz, BR = 1.2 kb/s	-	-119	-	dBm
		FDA = 5 kHz, BR = 4.8 kb/s	-	-115	-	dBm
		FDA = 40 kHz, BR = 38.4 kb/s*	-	-105	-	dBm
		FDA = 20 kHz, BR = 38.4 kb/s**	-	-105	-	dBm
		FDA = 62.5 kHz, BR = 250 kb/s***	-	-92	-	dBm
	Split RF paths, LnaBoost is turned on, the RF switch insertion loss is not accounted for. Band 3 /868/915	FDA = 5 kHz, BR = 1.2 kb/s	-	-123	-	dBm
		FDA = 5 kHz, BR = 4.8 kb/s	-	-119	-	dBm
		FDA = 40 kHz, BR = 38.4 kb/s*	-	-109	-	dBm
		FDA = 20 kHz, BR = 38.4 kb/s**	-	-109	-	dBm
		FDA = 62.5 kHz, BR = 250 kb/s***	-	-96	-	dBm
RFS_O	OOK sensitivity, highest LNA gain shared Rx, Tx paths	BR = 4.8 kb/s BR = 32 kb/s	-	-117 -108	-	dBm dBm
CCR	Co-Channel Rejection		-	-9	-	dB
ACR	Adjacent Channel Rejection	FDA = 5 kHz, BR = 4.8kb/s Offset = +/- 25 kHz or Offset = +/- 50 kHz				
		Band 1 Band 2	- -	50 56	- -	dB dB
BI_LF	Blocking Immunity Bands 1&2 /169/433	Offset = +/- 1 MHz	-	71	-	dB
		Offset = +/- 2 MHz	-	72	-	dB
		Offset = +/- 10 MHz	-	84	-	dB
BI_HF	Blocking Immunity Band 3 /868/915	Offset = +/- 1 MHz	-	71	-	dB
		Offset = +/- 2 MHz	-	76	-	dB
		Offset = +/- 10 MHz	-	84	-	dB
AMR	AM Rejection, AM modulated interfere with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz	-	73	-	dB
		Offset = +/- 2 MHz	-	78	-	dB
		Offset = +/- 10 MHz	-	87	-	dB
IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Highest LNA gain	-	+55	-	dBm
IIP3_LF	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Band 1	-	-22	-	dBm
		Highest LNA gain G1	-	-15	-	dBm
		LNA gain G2, 2.5dB sensitivity hit				
		Band 2	-	12.5	-	dBm
		Highest LNA gain G1	-	-8	-	dBm
		LNA gain G2, 2.5dB sensitivity hit				

WIRELESS PRODUCTS

Symbol	Description	Conditions	Min	Typ	Max	Unit
IIP3_HF	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Band 3 Highest LNA gain G1 LNA gain G2, 5dB sensitivity hit	-	-11	-	dBm
BW_SSB	Single Side channel filter BW	Programmable	2.7	-	250	kHz
IMR	Image Rejection	Wanted signal 3dB over sens BER=0.1%	-	50	-	dB
IMA	Image Attenuation		-	57	-	dB
DR_RSSI	RSSI Dynamic Range	AGC enabled	-127		0	dBm

Table 6

* $RxBw = 83 \text{ kHz}$ (Single Side Bandwidth)

** $RxBw = 50 \text{ kHz}$ (Single Side Bandwidth)

*** $RxBw = 250 \text{ kHz}$ (Single Side Bandwidth)

3.4. FSK/OOK MODE TRANSMITTER SPECIFICATION

Symbol	Description	Conditions	Min	Typ	Max	Unit
RF_OP	RF output power in 50 ohms on RFO pin (High efficiency PA).	Programmable with steps Max Min	+11 -	+14 -1	- -	dBm dBm
ΔRF_OP_V	RF output power stability on RFO pin versus voltage supply.	VDD = 2.5 V to 3.3 V VDD = 1.8 V to 3.7 V	- -	3 8	- -	dB dB
RF_OPH	RF output power in 50 ohms, on PA_BOOST pin (Regulated PA).	Programmable with 1dB steps Max Min	- -	+17 +2	- -	dBm dBm
RF_OPH_MAX	Max RF output power, on PA_BOOST pin	High power mode	-	+20	-	dBm
ΔRF_OPH_V	RF output power stability on PA_BOOST pin versus voltage supply.	VDD = 2.4 V to 3.7 V	-	+/-1	-	dB
ΔRF_T	RF output power stability versus temperature on both RF pins.	From T = -40 °C to +85 °C	-	+/-1	-	dB
PHN	Transmitter Phase Noise	169 MHz, Band 1				
		10kHz Offset	-	-118	-	dBc/Hz
		50kHz Offset	-	-118	-	
		400kHz Offset	-	-128	-	
		1MHz Offset	-	-134	-	
		433 MHz, Band 2				
		10kHz Offset	-	-110	-	dBc/Hz
		50kHz Offset	-	-110	-	
		400kHz Offset	-	-122	-	
1MHz Offset	-	-129	-			
868/915 MHz, Band 3						
10kHz Offset	-	-103	-	dBc/Hz		
50kHz Offset	-	-103	-			
400kHz Offset	-	-115	-			
1MHz Offset	-	-122	-			
ACP	Transmitter adjacent channel power (measured at 25 kHz offset)	BT=1. Measurement conditions as defined by EN 300 220-1 V2.3.1	-	-	-37	dBm
TS_TR	Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, PaRamp = 10us, BR = 4.8 kb/s	-	120	-	µs

Table 7

WIRELESS PRODUCTS

3.5. ELECTRICAL SPECIFICATION FOR LoRa™ MODULATION

The table below gives the electrical specifications for the transceiver operating with LoRa™ modulation. Following conditions apply unless otherwise specified:

- Supply voltage = 3.3 V.
- Temperature = 25° C.
- f_{XOSC} = 32 MHz.
- Bandwidth (BW) = 125 kHz.
- Spreading Factor (SF) = 12.
- Error Correction Code (EC) = 4/6.
- Packet Error Rate (PER)= 1%.
- CRC on payload enabled.
- Output power = 13 dBm in transmission.
- Payload length = 64bytes
- Preamble Length = 12 symbols (programmed register *PreambleLength* = 8)
- With matched impedances.

Electrical specifications: LoRa™ mode

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDR_L	Supply current in receiver LoRa™ mode, LnaBoost Off, Band1&2/169/433	BW = 7.8 kHz to 62.5 kHz	-	11.0	-	mA
		BW = 125 kHz	-	11.5	-	mA
		BW = 250 kHz	-	12.4	-	mA
		BW = 500 kHz	-	13.8	-	mA
IDDR_L	Supply current in receiver LoRa™ mode, LnaBoost Off, Band3/868/915	BW = 7.8 kHz to 62.5 kHz	-	9.9	-	mA
		BW = 125 kHz	-	10.3	-	mA
		BW = 250 kHz	-	11.1	-	mA
		BW = 500 kHz	-	12.6	-	mA
IDDT_L	Supply current in transmitter mode	RFOP = 13 dBm RFOP = 7 dBm	- -	28 20	- -	mA mA
IDDT_H_L	Supply current in transmitter mode with an external impedance transformation	Using PA_BOOST pin RFOP = 17 dBm	-	90	-	mA
BI_L	Blocking immunity, CW interferer	offset = +/- 1 MHz	-	89	-	dB
		offset = +/- 2 MHz	-	94	-	dB
		offset = +/- 10 MHz	-	100	-	dB
IIP2_L	2nd order input intercept point Unwanted tones are 20 MHz above the LO	Highest LNA gain	-	+55	-	dBm
IIP3_L_LF	3rd order input intercept point Unwanted tones are 1MHz and 1.995MHz above the LO	Band 1&2 Highest LNA gain G1	-	-22	-	dBm
		LNA gain G2,2.5dB sensitivity hit	-	-15	-	dBm
IIP3_L_HF	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Band 3 Highest LNA gain G1	-	-11	-	dBm
		LNA gain G2,2.5dB sensitivity hit	-	-6	-	dBm
BR_L	Bit rate, Long-Range Mode	From SF6, CR = 4/5, BW = 500 kHz to SF12, CR = 4/8, BW = 125 kHz	0.24	-	37.5	kbps
RFS_L7.8_LF	RF sensitivity, Long-Range Mode, highest LNA gain, Band 2 or 3, using split Rx/Tx path 7.8 kHz bandwidth	SF = 12	-	-148	-	dBm
		SF = 11	-	-145	-	dBm
RFS_L10_LF	RF sensitivity, Long-Range Mode, highest LNA gain, Band 3, 10.4 kHz bandwidth	SF = 6	-	-132	-	dBm
		SF = 7	-	-136	-	dBm
		SF = 8	-	-138	-	dBm
RFS_L62_LF	RF sensitivity, Long-Range Mode, highest LNA gain, Band 3, 62.5 kHz bandwidth	SF = 6	-	-123	-	dBm
		SF = 7	-	-128	-	dBm
		SF = 8	-	-131	-	dBm
		SF = 9	-	-134	-	dBm
		SF = 10	-	-135	-	dBm
		SF = 11	-	-137	-	dBm
SF = 12	-	-140	-	dBm		

WIRELESS PRODUCTS

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_L125_LF	RF sensitivity, Long-Range Mode, highest LNA gain, Band 3, 125 kHz bandwidth	SF = 6	-	-121	-	dBm
		SF = 7	-	-125	-	dBm
		SF = 8	-	-128	-	dBm
		SF = 9	-	-131	-	dBm
		SF = 10	-	-134	-	dBm
		SF = 11	-	-136	-	dBm
RFS_L250_LF	RF sensitivity, Long-Range Mode, highest LNA gain, Band 3 250 kHz bandwidth	SF = 6	-	-118	-	dBm
		SF = 7	-	-122	-	dBm
		SF = 8	-	-125	-	dBm
		SF = 9	-	-128	-	dBm
		SF = 10	-	-131	-	dBm
		SF = 11	-	-133	-	dBm
BR_L500_LF	RF sensitivity, Long-Range Mode, highest LNA gain, Band 3 500 kHz bandwidth	SF = 6	-	-112	-	dBm
		SF = 7	-	-118	-	dBm
		SF = 8	-	-121	-	dBm
		SF = 9	-	-124	-	dBm
		SF = 10	-	-127	-	dBm
		SF = 11	-	-129	-	dBm
RFS_L10_HF	RF sensitivity, Long-Range Mode, highest LNA gain, <i>LnaBoost</i> for Band 1, using split Rx/Tx path 10.4 kHz bandwidth	SF = 6	-	-131	-	dBm
		SF = 7	-	-134	-	dBm
		SF = 8	-	-138	-	dBm
		SF = 11	-	-146	-	dBm
RFS_L62_HF	RF sensitivity, Long-Range Mode, highest LNA gain, <i>LnaBoost</i> for Band 1, using split Rx/Tx path 62.5 kHz bandwidth	SF = 6	-	-121	-	dBm
		SF = 7	-	-126	-	dBm
		SF = 8	-	-129	-	dBm
		SF = 9	-	-132	-	dBm
		SF = 10	-	-135	-	dBm
		SF = 11	-	-137	-	dBm
RFS_L125_HF	RF sensitivity, Long-Range Mode, highest LNA gain, <i>LnaBoost</i> for Band 1, using split Rx/Tx path 125 kHz bandwidth	SF = 6	-	-118	-	dBm
		SF = 7	-	-123	-	dBm
		SF = 8	-	-126	-	dBm
		SF = 9	-	-129	-	dBm
		SF = 10	-	-132	-	dBm
		SF = 11	-	-133	-	dBm
RFS_L250_HF	RF sensitivity, Long-Range Mode, highest LNA gain, <i>LnaBoost</i> for Band 1, using split Rx/Tx path 250 kHz bandwidth	SF = 6	-	-115	-	dBm
		SF = 7	-	-120	-	dBm
		SF = 8	-	-123	-	dBm
		SF = 9	-	-125	-	dBm
		SF = 10	-	-128	-	dBm
		SF = 11	-	-130	-	dBm
RFS_L500_HF	RF sensitivity, Long-Range Mode, highest LNA gain, <i>LnaBoost</i> for Band 1, using split Rx/Tx path 500 kHz bandwidth	SF = 6	-	-111	-	dBm
		SF = 7	-	-116	-	dBm
		SF = 8	-	-119	-	dBm
		SF = 9	-	-122	-	dBm
		SF = 10	-	-125	-	dBm
		SF = 11	-	-128	-	dBm
CCR_LL	Co-channel rejection	Interferer is a LoRa™ signal using same BW and same SF.		-6		dBm
		Pw = Sensitivity + 3 dB				

WIRELESS PRODUCTS

Symbol	Description	Conditions	Min	Typ	Max	Unit
ACR_LCW	Adjacent channel rejection	Interferer is 1.5*BW_L from the wanted signal center frequency 1% PER, Single CW tone = Sens + 3 dB SF = 7 SF = 12	-	60 72	-	dB dB
IMR_LCW	Image rejection after calibration	1% PER, Single CW tone = Sens +3 dB	-	66	-	dB
FERR_L	Maximum tolerated frequency offset between transmitter and receiver, no sensitivity degradation, SF6 thru 12	All BW, +/-25% of BW The tighter limit applies (see below)		+/- 25%		BW
	Maximum tolerated frequency offset between transmitter and receiver, no sensitivity degradation, SF10 thru 12	SF = 12	-50	-	50	ppm
		SF = 11	-100	-	100	ppm
		SF = 10	-200	-	200	ppm

Table 8

3.6. DIGITAL SPECIFICATION

Conditions: Temp = 25° C, VDD = 3.3 V, FXOSC = 32 MHz, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
V _{IH}	Digital input level high		0.8	-	-	VDD
V _{IL}	Digital input level low		-	-	0.2	VDD
V _{OH}	Digital output level high	I _{max} = 1 mA	0.9	-	-	VDD
V _{OL}	Digital output level low	I _{max} = -1 mA	-	-	0.1	VDD
F _{SCK}	SCK frequency		-	-	10	MHz
t _{ch}	SCK high time		50	-	-	ns
t _{cl}	SCK low time		50	-	-	ns
t _{rise}	SCK rise time		-	5	-	ns
t _{fall}	SCK fall time		-	5	-	ns
t _{setup}	MOSI setup time	From MOSI change to SCK rising edge.	30	-	-	ns
t _{hold}	MOSI hold time	From SCK rising edge to MOSI change.	20	-	-	ns
t _{nsetup}	NSS setup time	From NSS falling edge to SCK rising edge.	30	-	-	ns
t _{nhold}	NSS hold time	From SCK falling edge to NSS rising edge, normal mode.	100	-	-	ns
t _{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

Table 9

4. DP1276 FEATURES

The DP1276 is equipped with both standard FSK and long range spread spectrum (LoRa™) modems. Depending upon the mode selected either conventional OOK or FSK modulation may be employed or the LoRa™ spread spectrum modem.

4.1. LoRa™ MODEM

The LoRa™ modem uses a proprietary spread spectrum modulation technique. This modulation, in contrast to legacy modulation techniques, permits an increase in link budget and increased immunity to in-band interference. At the same time the frequency tolerance requirement of the crystal reference oscillator is relaxed - allowing a performance increase for a reduction in system cost.

WIRELESS PRODUCTS

4.2. FSK/OOK MODEM

In FSK/OOK mode the DP1276 can avail of standard modulation techniques including OOK, FSK, GFSK, MSK and GMSK. The DP1276 is especially suited to narrow band communication thanks the low-IF architecture employed and the built-in AFC functionality.

4.3. RF POWER AMPLIFIERS

PA1 and PA2 are both connected to pin PA_BOOST. There are two potential configurations of these power Amplifiers, fixed or programmable. In the fixed configuration they can deliver up to +20 dBm. In programmable Configuration they can provide from +17 dBm to +2 dBm in 1 dB programmable steps.

PaSelect	Mode	Power Range	Pout Formula
1	PA1 and PA2 combined on pin PA_BOOST	+2 to +17 dBm	+2 dBm + <i>OutputPower</i>
1	PA1+PA2 on PA_BOOST with high output power +20 dBm	+5 to +20 dBm	+5 dBm + <i>OutputPower</i>

Table 10 Power Amplifier Mode Selection Truth Table

Note:

- For +20 dBm restrictions on operation please consult the following section.
- To ensure correct operation at the highest power levels ensure that the current limiter OcpTrim is adjusted to permit delivery of the requisite supply current.

4.4. HIGH POWER +20 dBm OPERATION

The DP1276 has a high power +20 dBm capability on PA_BOOST pin, with the following settings:

Register	Address	Value for High Power	Default value PA0 or +17dBm	Description
<i>RegPaDac</i>	0x5A	0x87	0x84	High power PA control

Table 11 High Power Settings

Note:

- High Power settings must be turned off when using PA0
- The Over Current Protection limit should be adapted to the actual power level, in RegOcp

Specific Absolute Maximum Ratings and Operating Range restrictions apply to the +20 dBm operation. They are listed in Table 11 and Table 12.

Symbol	Description	Min	Max	Unit
DC_20dBm	Duty Cycle of transmission at +20 dBm output	-	1	%
VSWR_20dBm	Maximum VSWR at antenna port, +20 dBm output	-	3:1	-
VDDop_20dBm	Supply voltage, +20 dBm output	2.4	3.7	V

Table 12 Operating Range, +20dBm Operation

The duty cycle of transmission at +20 dBm is limited to 1%, with a maximum VSWR of 3:1 at antenna port, over the Standard operating range [-40;+85°C]. For any other operating condition, contact your Anylink representative.

4.5. RF_MOD/VDD PIN FUNKTION DESKRIPTION

The Function of PIN RF_MOD/VDD depends on the Module variant. For C169 it is VDD of TCXO and RF-Switch and can be turned off in sleep mode. For C433, C868 and C915 the Pin is used to power the RF-Switch so in Sleep mode it has to be switched off to achieve the low power consumption of 1 µA. The same applies for C169.

5. SPI INTERFACE

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

- **SINGLE access:** an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte.
- **BURST access:** the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. These modes are available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.
- **FIFO access:** if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

The figure below shows a typical SPI single access to a register.

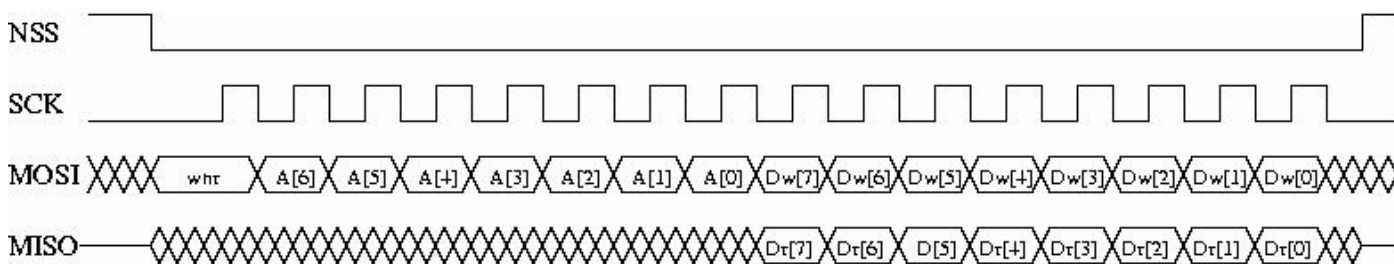


Figure 1 SPI Timing Diagram (single access)

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer is always started by the NSS pin going low. MISO is high impedance when NSS is high.

The first byte is the address byte. It is comprises:

- A wnr bit, which is 1 for write access and 0 for read access.
- Then 7 bits of address, MSB first.

The second byte is a data byte, either sent on MOSI by the master in case of a write access or received by the master on MISO in case of read access. The data byte is transmitted MSB first.

Proceeding bytes may be sent on MOSI (for write access) or received on MISO (for read access) without a rising NSS edge and re-sending the address. In FIFO mode, if the address was the FIFO address then the bytes will be written / read at the FIFO address. In Burst mode, if the address was not the FIFO address, then it is automatically incremented for each new byte received.

The frame ends when NSS goes high. The next frame must start with an address byte. The SINGLE access mode is therefore a special case of FIFO / BURST mode with only 1 data byte transferred.

During the write access, the byte transferred from the slave to the master on the MISO line is the value of the written register before the write operation.

6. INTRODUCTION TO THE LoRa™ MODEM AND ITS CAPABILITIES

The LoRa™ modem uses spread spectrum modulation and forward error correction techniques to increase the range and robustness of radio communication links compared to traditional FSK or OOK based modulation. Examples of the performance improvement possible, for several possible settings, are summarized in the table below. Here the spreading factor and error correction rate are design variables that allow the designer to optimize the trade-off between occupied bandwidth, data rate, link budget improvement and immunity to interference.

Bandwidth (kHz)	Spreading Factor	Coding rate	Nominal Rb (bps)	Sensitivity (dBm)	Module variant
10.4	6	4/5	782	-131	169
	12	4/5	24	-147	
20.8	6	4/5	1562	-128	
	12	4/5	49	-144	
62.5	6	4/5	4688	-121	169/433/868/915
	12	4/5	146	-139	
125	7	4/5	5469	-124	
	12	4/5	293	-136	
250	7	4/5	10938	-120	433/868/915
	12	4/5	586	-133	
500	7	4/5	21875	-117	
	12	4/5	1172	-130	

Table 13 Example LoRa™ Modem Performances

Notes - for all bandwidths lower than 62.5 kHz, it is advised to use a TCXO as a frequency reference. This is required to meet the frequency error tolerance specifications given in the Electrical Specification

- Higher spreading factors and longer transmission times impose more stringent constraints on the short term frequency stability of the reference. Please get in touch with a Anylink / Semtech representative to implement extremely low sensitivity products.

For European operation the range of crystal tolerances acceptable for each sub-band (of the ERC 70-03) is given in the specifications table. For US based operation a frequency hopping mode is available that automates both the LoRa™ spread spectrum and frequency hopping spread spectrum processes.

Another important facet of the LoRa™ modem is its increased immunity to interference. The LoRa™ modem is capable of co-channel GMSK rejection of up to 25 dB. This immunity to interference permits the simple coexistence of LoRa™ modulated systems either in bands of heavy spectral usage or in hybrid communication networks that use LoRa™ to extend range when legacy modulation schemes fail.

7. LINK DESIGN USING THE LoRa™ MODEM

7.1. OVERVIEW

The LoRa™ modem is setup as shown in the following figure. This configuration permits the simple replacement of the FSK modem with the LoRa™ modem via the configuration register setting RegOpMode. This change can be performed on the fly (in Sleep operating mode) thus permitting the use of both standard FSK or OOK in conjunction with the long range capability. The LoRa™ modulation and demodulation process is proprietary, it uses a form of spread spectrum modulation combined with cyclic error correction coding. The combined influence of these two factors is an increase in link budget and enhanced immunity to interference.

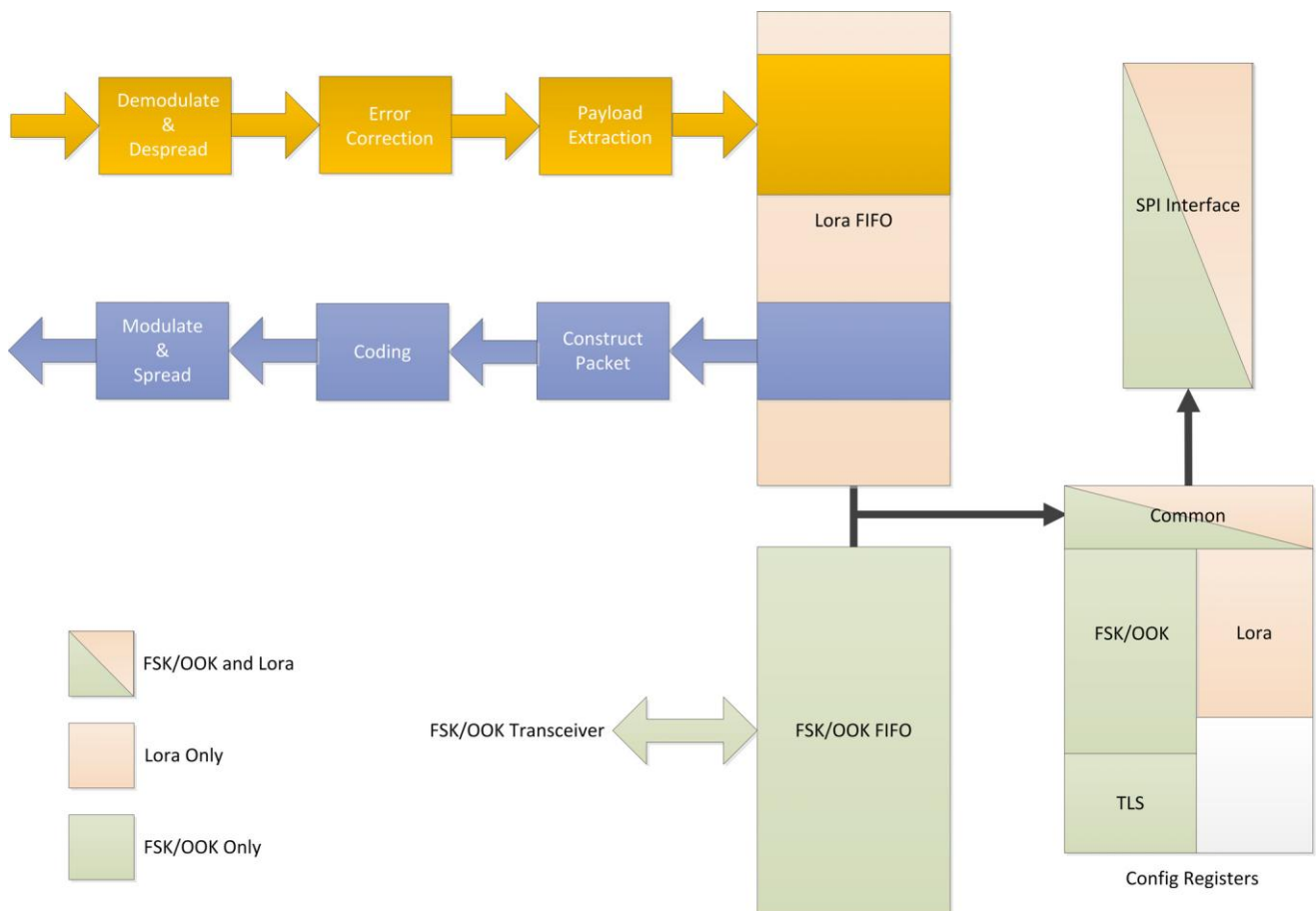


Figure 2 LoRa™ Modem Connectivity

A simplified outline of the transmit and receive processes is also shown above. Here we see that the LoRa™ modem has an independent dual port data buffer FIFO that is accessed through the SPI interface common to all modes. Upon selection of LoRa™ mode, the configuration register mapping of the DP1276 changes. For full details of this change please consult the register description of Semtech SX1276 Datasheet. (www.semtech.com)

So that it is possible to optimize the LoRa™ modulation for a given application, access is given to the designer to three critical design parameters. Each one permitting a tradeoff between link budget, immunity to interference, spectral occupancy and nominal data rate. These parameters are spreading factor, modulation bandwidth and error coding rate.

7.2. SPREADING FACTOR

The spread spectrum LoRa™ modulation is performed by representing each bit of payload information by multiple chips of information. The rate at which the spread information is sent is referred to as the symbol rate (R_s), the ratio between the nominal symbol rate and chip rate is the spreading factor and represents the number of symbols sent per bit of information. The range of values accessible with the LoRa™ modem are shown in the following table.

SpreadingFactor (RegModulationCfg)	Spreading Factor (Chips / symbol)	LoRa™ Demodulator SNR
6	64	-5 dB
7	128	-7.5 dB
8	256	-10 dB
9	512	-12.5 dB
10	1024	-15 dB
11	2048	-17.5 dB
12	4096	-20 dB

Table 14 Range of Spreading Factors

Note that the spreading factor, *SpreadingFactor*, must be known in advance on both transmit and receive sides of the link as different spreading factors are orthogonal to each other. Note also the resulting signal to noise ratio (SNR) required at the receiver input. It is the capability to receive signals with negative SNR that increases the sensitivity, so link budget and range, of the LoRa™ receiver.

Spreading Factor 6

SF = 6 is a special use case for the highest data rate transmission possible with the LoRa™ modem. To this end several settings must be activated in the SX1276/77/78 registers when it is in use:

- Set *SpreadingFactor* = 6 in *RegModemConfig2*
- The header must be set to Implicit mode
- Write bits 2-0 of register address 0x31 to value "0b101"
- Write register address 0x37 to value 0x0C

7.3. CODING RATE

To further improve the robustness of the link the LoRa™ modem employs cyclic error coding to perform forward error detection and correction. Such error coding incurs a transmission overhead - the resultant additional data overhead per transmission is shown in the table below.

CodingRate (RegTxCfg1)	Cyclic Coding Rate	Overhead Ratio
1	4/5	1.25
2	4/6	1.5
3	4/7	1.75
4	4/8	2

Table 15 Cyclic Coding Overhead

Forward error correction is particularly efficient in improving the reliability of the link in the presence of interference. So that the coding rate (and so robustness to interference) can be changed in response to channel conditions - the coding rate can optionally be included in the packet header for use by the receiver.

7.4. SIGNAL BANDWIDTH

An increase in signal bandwidth permits the use of a higher effective data rate, thus reducing transmission time at the expense of reduced sensitivity improvement. There are of course regulatory constraints in most countries on the permissible occupied bandwidth. Contrary to the FSK modem which is described in terms of the single sideband bandwidth, the LoRa™ modem bandwidth refers to the double sideband bandwidth (or total channel bandwidth). The range of bandwidths relevant to most regulatory situations is given in the LoRa™ modem specifications Table 8 on Page 9.

Bandwidth (kHz)	Spreading Factor	Coding rate	Nominal Rb (bps)
7.8	12	4/5	18
10.4	12	4/5	24
15.6	12	4/5	37
20.8	12	4/5	49
31.2	12	4/5	73
41.7	12	4/5	98
62.5	12	4/5	146
125	12	4/5	293
250	12	4/5	586
500	12	4/5	1172

Table 16 LoRa™ Bandwidth Options

Note: In the lower band (169 MHz), the 250 kHz and 500 kHz bandwidths are not supported.

7.5. LoRa™ TRANSMISSION PARAMETER RELATIONSHIP

With knowledge of the key parameters that can be controlled by the user we define the LoRa™ symbol rate as:

$$R_s = \frac{BW}{2^{SF}}$$

where BW is the programmed bandwidth and SF is the spreading factor. The transmitted signal is a constant envelope signal. Equivalently, one chip is sent per second per Hz of bandwidth.

7.6. LoRa™ PACKET STRUCTURE

The LoRa™ modem employs two types of packet format, explicit and implicit. The explicit packet includes a short header that contains information about the number of bytes, coding rate and whether a CRC is used in the packet. The packet format is shown in the following figure.

The LoRa™ packet comprises three elements:

- A preamble.
- An optional header.
- The data payload.

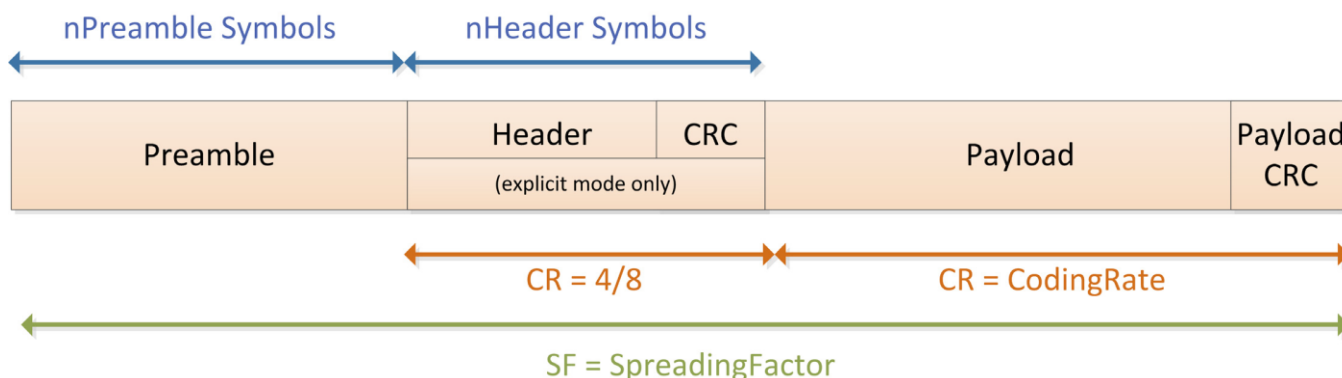


Figure 3 LoRa™ Packet Structure

7.6.1. PREAMBLE

The preamble is used to synchronize receiver with the incoming data flow. Although by default, it consists of a 12 symbol long sequence - the receiver does not require knowledge of the preamble length. The preamble length may be extended in the interest of reducing to receiver duty cycle in receive intensive applications. However, the minimum length suffices for all communication. The transmitted preamble length may be changed by setting the register PreambleLength from 12 to 32768.

7.6.2. HEADER

Depending upon the chosen mode of operation two types of header are available. The header type is selected by the ImplicitHeaderMode bit found within the RegSymbTimeoutMsb register.

7.6.2.1. EXPLICIT HEADER MODE

This is the default mode of operation. Here the header provides information on the payload, namely:

- The payload length in bytes.
- The forward error correction code rate
- The presence of an optional 16-bits CRC for the payload.

The header is transmitted with maximum error correction code (4/8). It also has its own CRC to allow the receiver to discard invalid headers.

7.6.3. IMPLICIT HEADER MODE

In certain scenarios, where the payload, coding rate and CRC presence are fixed or known in advance, it may be advantageous to reduce transmission time by invoking implicit header mode. In this mode the header is removed from the packet. In this case the payload length, error coding rate and presence of the payload CRC must be manually configured on both sides of the radio link.

7.6.4. PAYLOAD

The packet payload is a variable-length field that contains the actual data coded at the error rate either as specified in the header in explicit mode or in the register settings in implicit mode. An optional CRC may be appended.

7.7. TIME ON AIR

For a given combination of spreading factor (SF), coding rate (CR) and signal bandwidth (BW) the total on-the-air transmission time of a LoRa™ packet can be calculated as follows. From the definition of the symbol rate it is convenient to define the symbol rate:

$$T_s = \frac{1}{R_s}$$

The LoRa™ packet duration is the sum of the duration of the preamble and the transmitted packet. The preamble length is calculated as follows:

$$T_{preamble} = (n_{preamble} + 4.25)T_{sym}$$

where $n_{preamble}$ is the programmed preamble length, taken from the registers *RegPreambleMsb* and *RegPreambleLsb*. The payload duration depends upon the header mode that is enabled. The following formula gives the number of payload symbols.

$$\text{payloadSymbNb} = 8 + \max\left(\text{ceil}\left(\frac{8\text{PL} - 4\text{SF} + 16 - 20\text{H}}{4(\text{SF} - 2\text{DE})}\right)(\text{CR} + 4), 0\right)$$

With the following dependencies:

- PL is the number of Payload bytes
- SF is the spreading factor
- H=0 when the header is enabled, H=1 when no header is present
- DE=1 when LowDataRateOptimize=1, DE=0 otherwise
- CR is the coding rate from 1 to 4

The Payload duration is then the symbol period multiplied by the number of Payload symbols

$$T_{payload} = \text{payloadSymbNb}T_{sym}$$

The time on air, or packet duration, is simply then the sum of the preamble and payload duration.

$$T_{packet} = T_{preamble} + T_{payload}$$

7.8. FREQUENCY HOPPING WITH LoRa™

The duration of a single packet could exceed regulatory requirements relating to the maximum permissible channel dwell time. To ease implementation and ensure continued compliance when operating in frequency hopping spread spectrum (FHSS) mode (FhssMode of register *RegTxCfg1*) can be enabled.

7.8.1. PRINCIPLE OF OPERATION

The principle behind the FHSS scheme is that a portion of each LoRa™ packet is transmitted on each hopping channel from a look up table of frequencies managed by the host microcontroller. After a predetermined hopping period the transmitter changes to the next channel in a predefined list of hopping frequencies and continues transmitting the next symbol of the packet. The time which the transmission will last in any given channel is determined by HoppingPeriod which is an integer multiple of symbol periods:

$$HoppingPeriod = TS \times FreqHoppingPeriod$$

The frequency hopping transmission and reception process starts at channel 0, following each frequency hop the channel counter stored in FhssPresentChannel is incremented and the interrupt signal FhssChangeChannel is generated. Upon completion of the transmission on any given channel the companion microcontroller must hence read the FhssPresentChannel value and load the corresponding RF centre frequency into the Frf register.

FHSS Reception always starts on channel 0. The receiver waits for a valid preamble detection before starting the frequency hopping process as described above. Note that in the eventuality of header CRC corruption, the receiver will automatically request channel 0 and recommence the valid preamble detection process.

7.8.2. TIMING OF CHANNEL UPDATES

The interrupt requesting the channel change, FhssChannelChange, is generated at least 1 ms before the next frequency value must be written - allowing ample time for most MCUs to update the register. The frequency hopping process is recapitulated in the diagram below:

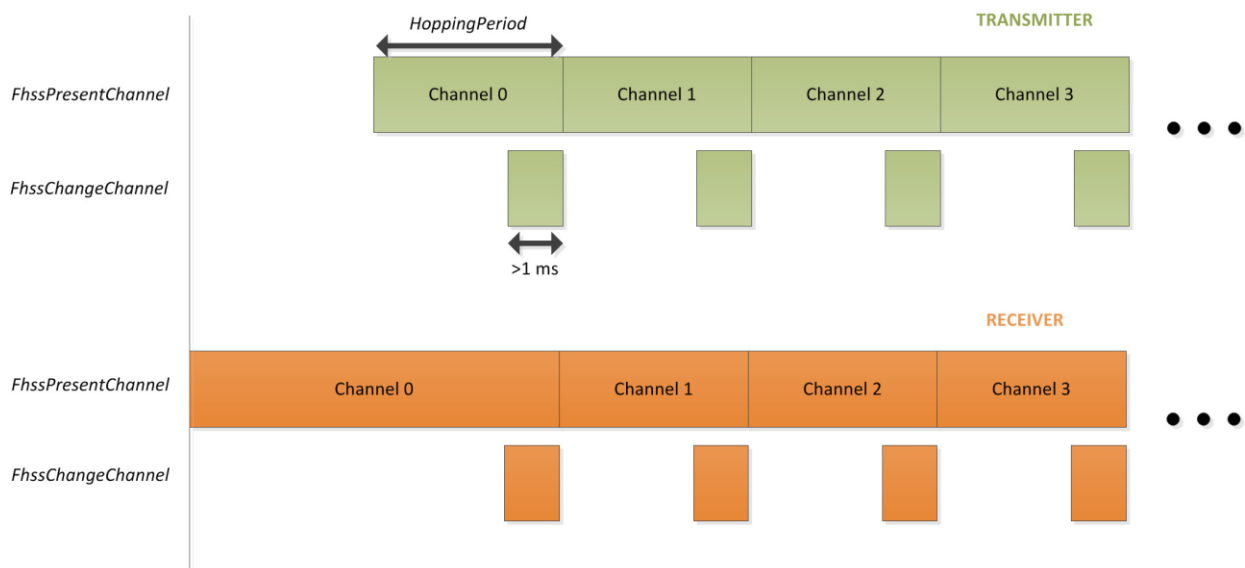


Figure 4 Interrupts generated in the case of successful frequency hopping communication

8. FSK/OOK MODEM

8.1. BIT RATE SETTING

The bitrate setting is referenced to the crystal oscillator and provides a precise means of setting the bit rate (or equivalently chip) rate of the radio. In continuous transmit mode the data stream to be transmitted can be input directly to the modulator via pin 9 (DIO2/DATA) in an asynchronous manner, unless Gaussian filtering is used, in which case the DCLK signal on pin 8 (DIO1/DCLK) is used to synchronize the data stream.

In Packet mode or in Continuous mode with Gaussian filtering enabled, the Bit Rate (BR) is controlled by bits Bitrate in RegBitrateMsb and RegBitrateLsb

$$BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$$

Note: BitrateFrac bits have no effect (i.e may be considered equal to 0) in OOK modulation mode.

The quantity BitrateFrac is hence designed to allow very high precision (max. 250 ppm programming resolution) for any bitrate in the programmable range. Table 24 below shows a range of standard bitrates and the accuracy to within which they may be reached.

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical modem baud rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps		38415.36
	0x01	0xA1	76.8 kbps		76738.60
Classical modem baud rates (multiples of 0.9 kbps)	0x00	0xD0	153.6 kbps		153846.1
	0x02	0x2C	57.6 kbps		57553.95
Round bit rates (multiples of 12.5, 25 and 50 kbps)	0x01	0x16	115.2 kbps		115107.9
	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x80	0x00	50 kbps		50000.00
	0x01	0x40	100 kbps		100000.0
	0x00	0xD5	150 kbps		150234.7
	0x00	0xA0	200 kbps		200000.0
Watch Xtal frequency	0x00	0x80	250 kbps		250000.0
	0x00	0x6B	300 kbps		299065.4
Watch Xtal frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

Table 17 Bit Rate Examples

9. OPERATING MODES IN FSK/OOK MODE

9.1. GENERAL OVERVIEW

The DP1276 has several working modes, manually programmed in RegOpMode. Fully automated mode selection, packet transmission and reception is also possible using the Top Level Sequencer described in Section 11.5.

Mode	Selected mode	Symbol	Enabled blocks
000	Sleep mode	Sleep	None
001	Standby mode	Stdby	Top regulator and crystal oscillator
010	Frequency synthesiser to Tx frequency	FSTx	Frequency synthesizer at Tx frequency (Frf)
011	Transmit mode	Tx	Frequency synthesizer and transmitter
100	Frequency synthesiser to Rx frequency	FSRx	Frequency synthesizer at frequency for reception (Frf-IF)
101	Receive mode	Rx	Frequency synthesizer and receiver

Table 18 Basic Transceiver Modes

When switching from a mode to another the sub-blocks are woken up according to a pre-defined optimized sequence.

9.2. STARTUP TIMES

The startup time of the transmitter or the receiver is dependent upon which mode the transceiver was in at the beginning.

For a complete description, Figure 6 below shows a complete startup process, from the lower power mode "Sleep".

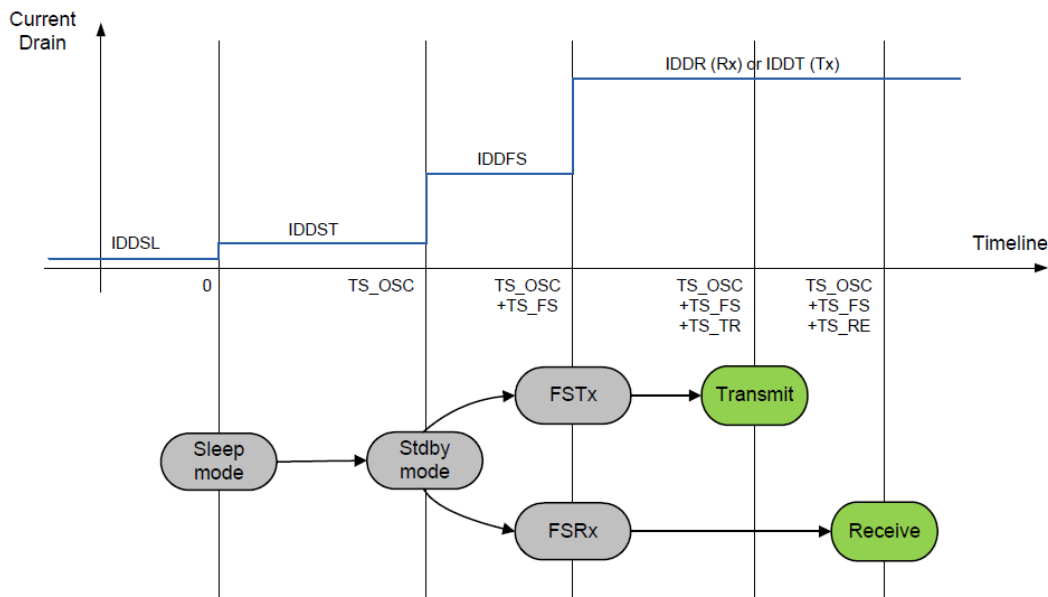


Figure 5 Startup Process

TS_OSC is the startup time of the crystal oscillator which depends on the electrical characteristics of the crystal. TS_FS is the startup time of the PLL including systematic calibration of the VCO.

9.2.1. TRANSMITTER STARTUP TIME

The transmitter startup time, TS_{TR} , is calculated as follows in FSK mode:

$$TS_{TR} = 5\mu s + 1.25 * PaRamp + \frac{1}{2} * Tbit$$

- PaRamp is the ramp-up time programmed in RegPaRamp.
- Tbit is the bit time.

In OOK mode, this equation can be simplified to the following:

$$TS_{TR} = 5\mu s + \frac{1}{2} * Tbit$$

9.2.2. RECEIVER STARTUP TIME

The receiver startup time, TS_{RE} , only depends upon the receiver bandwidth effective at the time of startup. When AFC is enabled (AfcAutoOn=1), AfcBw should be used instead of RxBw to extract the receiver startup time:

RxBw if AfcAutoOn=0 RxBwAfc if AfcAutoOn=1	TS_RE (+/-5%)
2.6 kHz	2.33 ms
3.1 kHz	1.94 ms
3.9 kHz	1.56 ms
5.2 kHz	1.18 ms
6.3 kHz	984 μs
7.8 kHz	791 μs
10.4 kHz	601 μs
12.5 kHz	504 μs
15.6 kHz	407 μs
20.8 kHz	313 μs
25.0 kHz	264 μs
31.3 kHz	215 μs
41.7 kHz	169 μs
50.0 kHz	144 μs
62.5 kHz	119 μs
83.3 kHz	97 μs
100.0 kHz	84 μs
125.0 kHz	71 μs
166.7 kHz	85 μs
200.0 kHz	74 μs
250.0 kHz	63 μs

Table 19 Receiver Startup Time Summary

TS_{RE} or later after setting the device in Receive mode, any incoming packet will be detected and demodulated by the transceiver.

9.2.3. TIME TO RSSI EVALUATION

The first RSSI sample will be available TS_RSSI after the receiver is ready, in other words TS_RE + TS_RSSI after the receiver was requested to turn on.

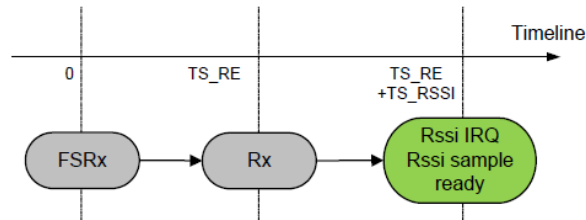
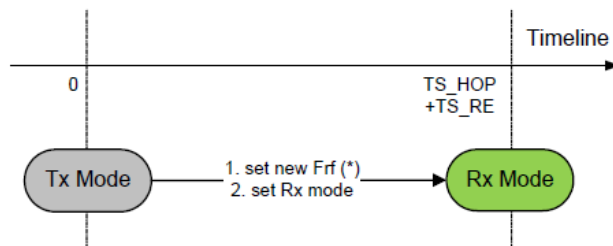


Figure 6 Time to Rssi Sample

TS_RSSI depends on the receiver bandwidth, as well as the *RssiSmoothing* option that was selected.

9.2.4. TX TO RX TURNAROUND TIME

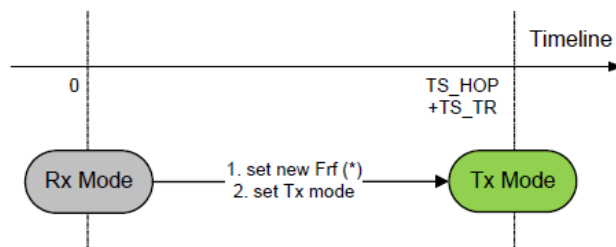


(*) Optional

Figure 7 Tx to Rx Turnaround

Note The SPI instruction times are omitted, as they can generally be very small as compared to other timings (up to 10MHz SPI clock).

9.2.5. RX TO TX



(*) Optional

Figure 8 Rx to Tx Turnaround

9.2.6. RECEIVER HOPPING; RX TO RX

Two methods are possible:

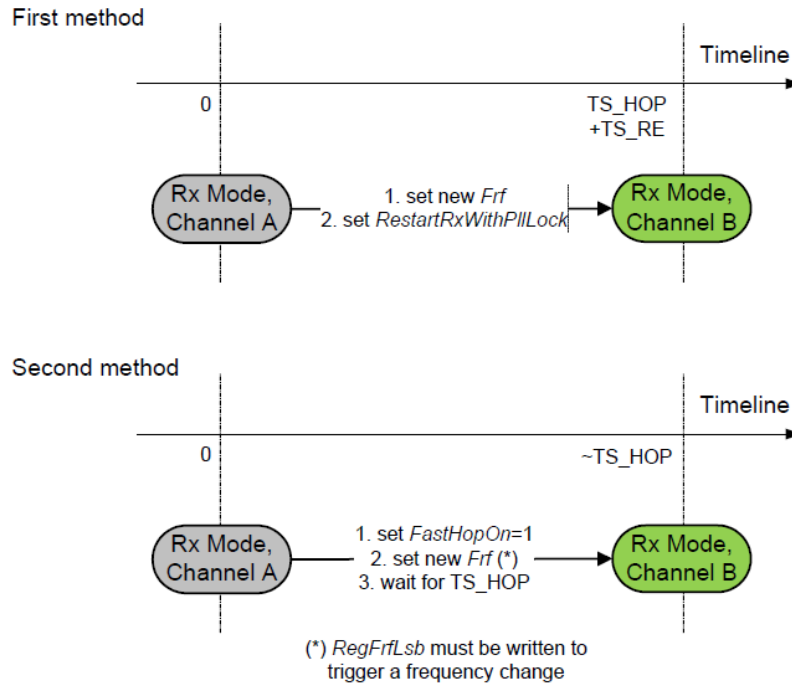


Figure 9 Receiver Hopping

The second method is quicker, and should be used if a very quick RF sniffing mechanism is to be implemented.

9.2.7. TX TO TX

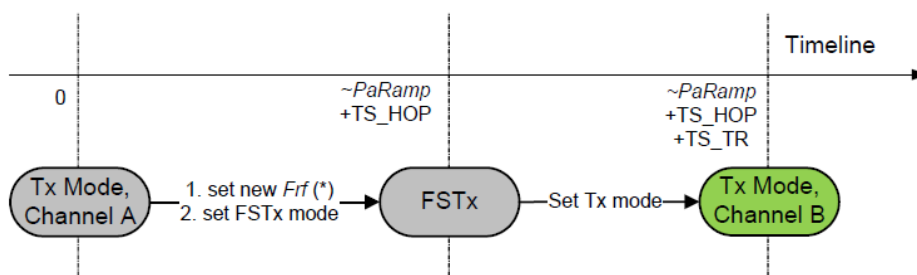


Figure 10 Transmitter Hopping

9.3. RECEIVER STARTUP OPTIONS

The DP1276 receiver can automatically control the gain of the receive chain (AGC) and adjust the receiver LO frequency (AFC). Those processes are carried out on a packet-by-packet basis. They occur:

- When the receiver is turned On.
- When the Receiver is restarted upon user request, through the use of trigger bits RestartRxWithoutPllLock or RestartRxWithPllLock, in RegRxConfig.
- When the receiver is automatically restarted after the reception of a valid packet, or after a packet collision.

The receiver startup options available in DP1276 are described in Table 18.

Triggering Event	Realized Function	AgcAutoOn	AfcAutoOn	RxTrigger (2:0)
None	None	0	0	000
Rssi Interrupt	AGC	1	0	001
	AGC & AFC	1	1	001
PreambleDetect	AGC	1	0	110
	AGC & AFC	1	1	110
Rssi Interrupt & PreambleDetect	AGC	1	0	111
	AGC & AFC	1	1	111

Table 20 Receiver Startup Options

When *AgcAutoOn*=0, the LNA gain is manually selected by choosing *LnaGain* bits in *RegLna*.

9.4. RECEIVER RESTART METHODS

The options for restart of the receiver are covered below. This is typically of use to prepare for the reception of a new signal whose strength or carrier frequency is different from the preceding packet to allow the AGC or AFC to be re-evaluated.

9.4.1. RESTART UPON USER REQUEST

In Receive mode the user can request a receiver restart - this can be useful in conjunction with the use of a Timeout interrupt following a period of inactivity in the channel of interest. Two options are available:

- No change in the Local Oscillator upon restart: the AFC is disabled, and the Frf register has not been changed through SPI before the restart instruction: set bit RestartRxWithoutPllLock in RegRxConfig to 1.
- Local Oscillator change upon restart: if AFC is enabled (*AfcAutoOn*=1), and/or the Frf register had been changed during the last Rx period: set bit RestartRxWithPllLock in RegRxConfig to 1.

Note ModeReady must be at logic level 1 for a new RestartRx command to be taken into account.

9.4.2. AUTOMATIC RESTART AFTER VALID PACKET RECEPTION

The bits AutoRestartRxMode in RegSyncConfig control the automatic restart feature of the DP1276 receiver, when a valid packet has been received:

- If AutoRestartRxMode = 00, the function is off, and the user should manually restart the receiver upon valid packet reception.
- If AutoRestartRxMode = 01, after the user has emptied the FIFO following a PayloadReady interrupt, the receiver will automatically restart itself after a delay of InterPacketRxDelay, allowing for the distant transmitter to ramp down, hence avoiding a false RSSI detection on the 'tail' of the previous packet.
- If AutoRestartRxMode = 10 should be used if the next reception is expected on a new frequency, i.e. Frf is changed after the reception of the previous packet. An additional delay is systematically added, in order for the PLL to lock at a new frequency.

9.4.3. AUTOMATIC RESTART WHEN PACKET COLLISION IS DETECTED

In receive mode the DP1276 is able to detect packet collision and restart the receiver. Collisions are detected by a sudden rise in received signal strength, detected by the RSSI. This functionality can be useful in network configurations where many asynchronous slaves attempt periodic communication with a single a master node.

The collision detector is enabled by setting bit `RestartRxOnCollision` to 1.

The decision to restart the receiver is based on the detection of RSSI change. The sensitivity of the system can be adjusted in 1 dB steps by using register `RssiCollisionThreshold` in `RegRxConfig`.

9.5. TOP LEVEL SEQUENCER

Depending on the application, it is desirable to be able to change the mode of the circuit according to a predefined sequence without access to the serial interface. In order to define different sequences or scenarios, a user-programmable state machine, called Top Level Sequencer (Sequencer in short), can automatically control the chip modes.

NOTE: THIS FUNCTIONALITY IS ONLY AVAILABLE IN FSK/OOK MODE.

The Sequencer is activated by setting the `SequencerStart` bit in `RegSeqConfig1` to 1 in Sleep or Standby mode (called initial mode).

It is also possible to force the Sequencer off by setting the `Stop` bit in `RegSeqConfig1` to 1 at any time.

Note: `SequencerStart` and `Stop` bit must never be set at the same time.

9.5.1. SEQUENCER STATES

As shown in the table below, with the aid of a pair of interrupt timers (T1 and T2), the sequencer can take control of the chip operation in all modes.

Sequencer State	Description
SequencerOff State	The Sequencer is not activated. Sending a <code>SequencerStart</code> command will launch it. When coming from LowPowerSelection state, the Sequencer will be Off, whilst the chip will return to its initial mode (either Sleep or Standby mode).
Idle State	The chip is in low-power mode, either <i>Standby</i> or <i>Sleep</i> , as defined by <code>IdleMode</code> in <code>RegSeqConfig1</code> . The Sequencer waits only for the <code>T1</code> interrupt.
Transmit State	The transmitter in on.
Receive State	The receiver in on.
PacketReceived	The receiver is on and a packet has been received. It is stored in the FIFO.
LowPowerSelection	Selects low power state (SequencerOff or Idle State)
RxTimeout	Defines the action to be taken on a <code>RxTimeout</code> interrupt. <code>RxTimeout</code> interrupt can be a <code>TimeoutRxRssi</code> , <code>TimeoutRxPreamble</code> or <code>TimeoutSignalSync</code> interrupt.

Table 21 Sequencer States

WIRELESS PRODUCTS

9.5.2. SEQUENCER TRANSITIONS

The transitions between sequencer states are listed in the forthcoming table.

Variable	Transition
<i>IdleMode</i>	Selects the chip mode during Idle state: 0: <i>Standby</i> mode 1: <i>Sleep</i> mode
<i>FromStart</i>	Controls the Sequencer transition when the <i>SequencerStart</i> bit is set to 1 in <i>Sleep</i> or <i>Standby</i> mode: 00: to LowPowerSelection 01: to Receive state 10: to Transmit state 11: to Transmit state on a <i>FifoThreshold</i> interrupt
<i>LowPowerSelection</i>	Selects Sequencer LowPower state after a <i>to LowPowerSelection</i> transition 0: SequencerOff state with chip on Initial mode 1: Idle state with chip on <i>Standby</i> or <i>Sleep</i> mode depending on IdleMode Note: Initial mode is the chip LowPower mode at Sequencer start.
<i>FromIdle</i>	Controls the Sequencer transition from the Idle state on a <i>T1</i> interrupt: 0: to Transmit state 1: to Receive state
<i>FromTransmit</i>	Controls the Sequencer transition from the Transmit state: 0: to LowPowerSelection on a <i>PacketSent</i> interrupt 1: to Receive state on a <i>PacketSent</i> interrupt
<i>FromReceive</i>	Controls the Sequencer transition from the Receive state: 000 and 111: unused 001: to PacketReceived state on a <i>PayloadReady</i> interrupt 010: to LowPowerSelection on a <i>PayloadReady</i> interrupt 011: to PacketReceived state on a <i>CrcOk</i> interrupt. If CRC is wrong (corrupted packet, with CRC on but <i>CrcAutoClearOn</i> is off), the <i>PayloadReady</i> interrupt will drive the sequencer to <i>RxTimeout</i> state. 100: to SequencerOff state on a <i>Rssi</i> interrupt 101: to SequencerOff state on a <i>SyncAddress</i> interrupt 110: to SequencerOff state on a <i>PreambleDetect</i> interrupt Irrespective of this setting, transition to LowPowerSelection on a <i>T2</i> interrupt
<i>FromRxTimeout</i>	Controls the state-machine transition from the Receive state on a <i>RxTimeout</i> interrupt (and on <i>PayloadReady</i> if FromReceive = 011): 00: to Receive state via <i>ReceiveRestart</i> 01: to Transmit state 10: to LowPowerSelection 11: to SequencerOff state Note: <i>RxTimeout</i> interrupt is a <i>TimeoutRxRssi</i> , <i>TimeoutRxPreamble</i> or <i>TimeoutSignalSync</i> interrupt.
<i>FromPacketReceived</i>	Controls the state-machine transition from the PacketReceived state: 000: to SequencerOff state 001: to Transmit on a <i>FifoEmpty</i> interrupt 010: to LowPowerSelection 011: to Receive via <i>FS</i> mode, if frequency was changed 100: to Receive state (no frequency change)

Table 22 Sequencer Transition Options

9.5.3. TIMERS

Two timers (Timer1 and Timer2) are also available in order to define periodic sequences. These timers are used to generate interrupts, which can trigger transitions of the Sequencer.

T1 interrupt is generated (Timer1Resolution * Timer1Coefficient) after T2 interrupt or SequencerStart. command.
T2 interrupt is generated (Timer2Resolution * Timer2Coefficient) after T1 interrupt.

The timers' mechanism is summarized on the following diagram.

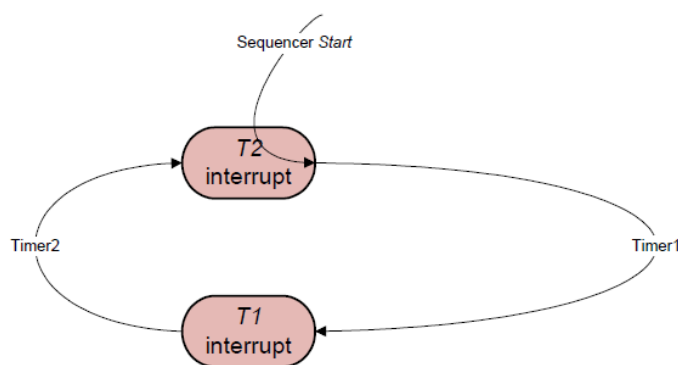


Figure 11 Timer1 and Timer2 Mechanism

Note: The timer sequence is completed independently of the actual Sequencer state. Thus, both timers need to be on to achieve periodic cycling.

Variable	Description
Timer1Resolution	Resolution of Timer1 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms
Timer2Resolution	Resolution of Timer2 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms
Timer1Coefficient	Multiplying coefficient for Timer1
Timer2Coefficient	Multiplying coefficient for Timer2

Table 23 Sequencer Timer Settings

9.5.4. SEQUENCER STATE MACHINE

The following graphs summarize every possible transition between each Sequencer state. The Sequencer states are highlighted in grey. The transitions are represented by arrows. The condition activating them is described over the transition arrow. For better readability, the start transitions are separated from the rest of the graph.

Transitory states are highlighted in light grey, and exit states are represented in red. It is also possible to force the Sequencer off by setting the Stop bit in RegSeqConfig1 to 1 at any time.

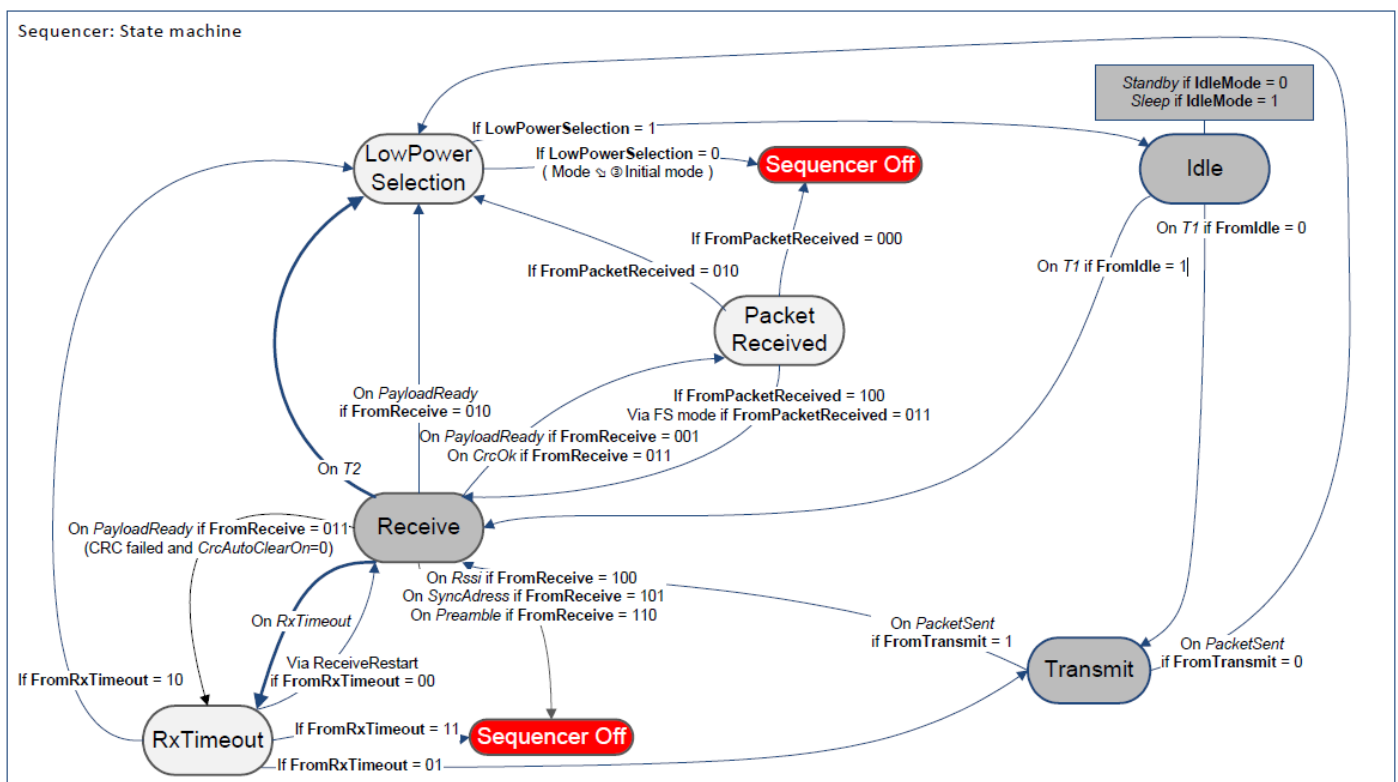
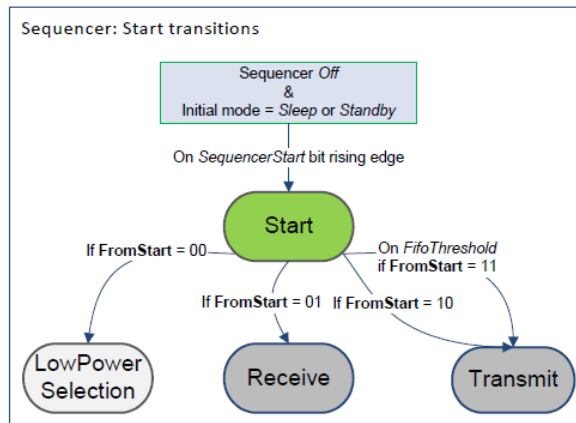


Figure 12 Sequencer State Machine

10. PACKET FORMAT

10.1. FIXED LENGTH PACKET FORMAT

Fixed length packet format is selected when bit PacketFormat is set to 0 and PayloadLength is set to any value greater than 0.

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes, whether Tx only, Rx only, or Tx/Rx should be programmed with the same packet length value.

The length of the payload is limited to 2047 bytes.

The length programmed in PayloadLength relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

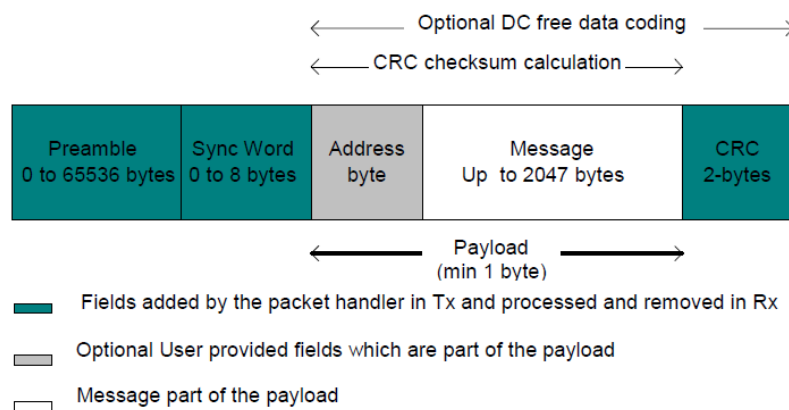


Figure 13 Fixed Length Packet Format

10.2. VARIABLE LENGTH PACKET FORMAT

Variable length packet format is selected when bit PacketFormat is set to 1.

This mode is useful in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.

In this mode the length of the payload, indicated by the length byte, is given by the first byte of the FIFO and is limited to 255 bytes. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Length byte
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

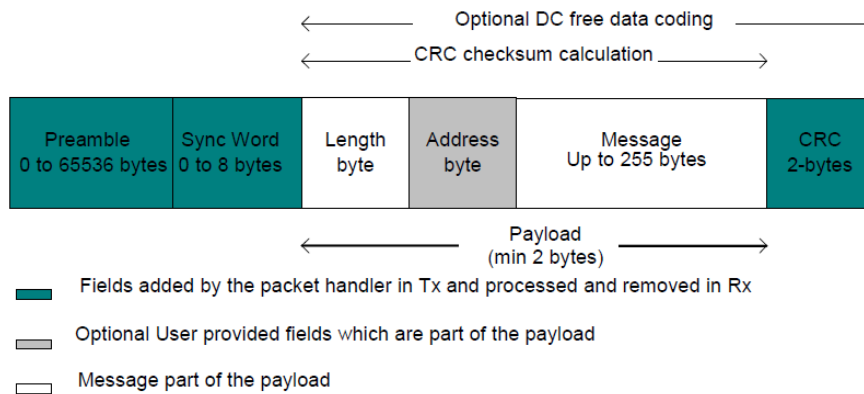


Figure 14 Variable Length Packet Format

10.3. UNLIMITED LENGTH PACKET FORMAT

Unlimited length packet format is selected when bit PacketFormat is set to 0 and PayloadLength is set to 0.

The user can then transmit and receive packet of arbitrary length and PayloadLength register is not used in Tx/Rx modes for counting the length of the bytes transmitted/received.

In Tx the data is transmitted depending on the TxStartCondition bit. On the Rx side the data processing features like Address filtering, Manchester encoding and data whitening are not available if the sync pattern length is set to zero (SyncOn = 0). The filling of the FIFO in this case can be controlled by the bit FifoFillCondition. The CRC detection in Rx is also not supported in this mode of the packet handler, however CRC generation in Tx is operational. The interrupts like CrcOk & PayloadReady are not available either.

An unlimited length packet shown below is made up of the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Optional Address byte (Node ID).
- Message data
- Optional 2-bytes CRC checksum (Tx only)

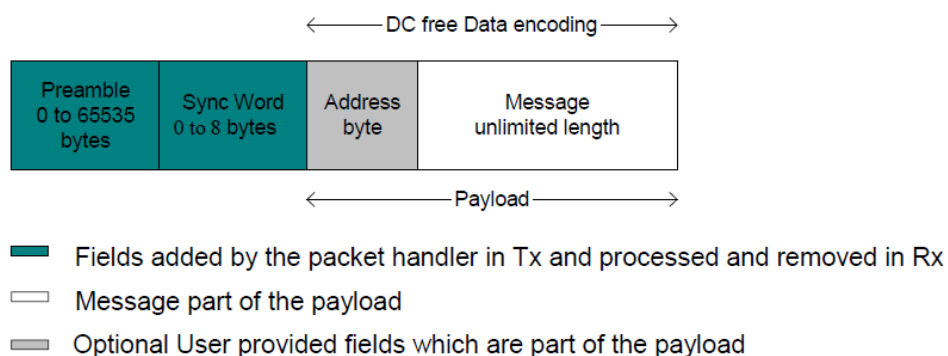
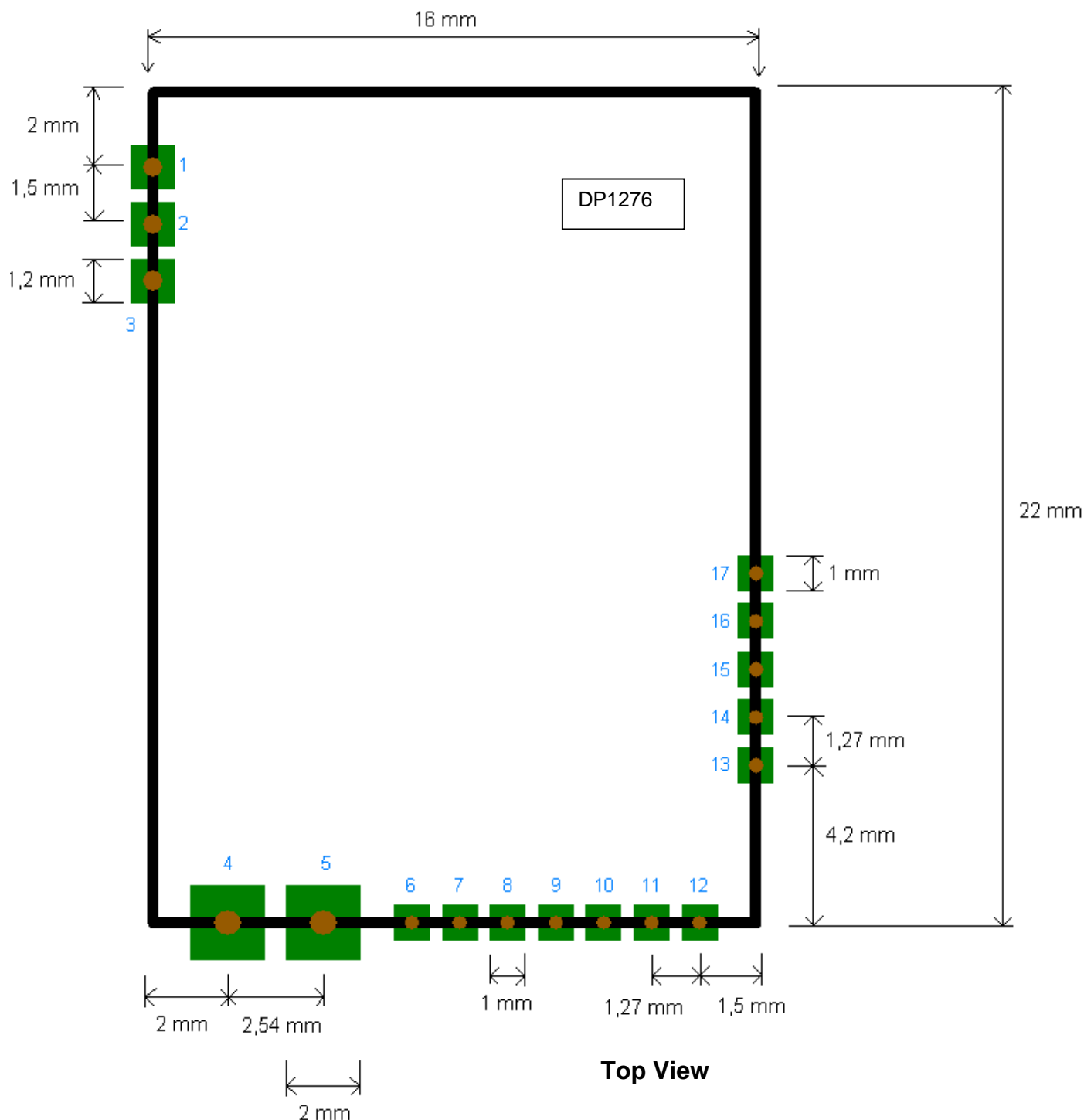


Figure 15 Unlimited Length Packet Format

11. MECHANICAL DIMENSIONS

The following drawing shows the physical footprint and dimensions of the DP1276 drop-in module.



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