DP1272 – C868/C915

860 MHz to 1020 MHz Low Power Long Range Transceiver

Combine Small Form Factor with High Performance

GENERAL DESCRIPTION

The DP1272 includes the LoRa™ long range modem that provides ultra-long range spread spectrum communication and high interference immunity whilst minimizing current consumption.

Using Semtech's patented LoRa™ modulation technique DP1272 can achieve sensitivity of over -137 dBm. The high sensitivity combined with the integrated +20 dBm power amplifier yields industry leading link budget making it optimal for any application requiring range or robustness. LoRa™ also provides significant advantages in blocking and selectivity over conventional modulation techniques. Solving the design compromise between range, interference immunity and energy consumption.

These devices also support high performance (G)FSK modes for Wireless M-Bus, IEEE802.15.4g and similar compatibility modes. The SX1272 deliver exceptional phase noise, selectivity, receiver linearity and IIP3 for significantly lower current consumption than competing devices.

APPLICATIONS

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control
- Long range Irrigation Systems

KEY PRODUCT FEATURES

- LoRa™ Modem.
- Automated Meter Reading.
- Home and Building Automation.
- Wireless Alarm and Security Systems.
- Industrial Monitoring and Control.
- 157.5 dB maximum link budget.
- +20dBm - 100mW constant RF output vs. V supply.
- +14 dBm high efficiency PA.
- Programmable bit rate up to 300 kbps.
- High sensitivity: down to -137.5 dBm.
- Bullet-proof front end: IIP3 = -12 dBm with FSK.
- 100 dB blocking immunity.
- Low RX current of 10 mA, 7µA register retention.
- Fully integrated synthesizer (resolution of 61Hz).
- FSK,GFSK,MSK,GMSK,LORA,OOK modulations.
- Built-in bit synchronizer for clock recovery
- Sync word recognition
- Preamble detection
- 127 dB+ Dynamic Range RSSI
- Automatic RF Sense with ultra-fast AFC
- Packet engine up to 256 bytes with CRC
- Built-in temperature sensor, low battery indicator
- IO-Home control mode

DEVICE OPTIONS

Part	Frequency band	Pin Package
DP1272C868	860 - 902 MHz	Board
DP1272C915	902 - 1020 MHz	Board

Table of Contents

1. PIN DESCRIPTION 4

2. ELECTRICAL CHARACTERISTICS 5

2.1. Absolute Maximum Ratings 5

2.2. OPERATING RANGE 5

3. SPECIFICATIONS 6

3.1. POWER CONSUMPTION SPECIFICATION 6

3.2. FREQUENCY SYNTHESIZER SPECIFICATION 6

3.3. FSK/OOK MODE RECEIVER SPECIFICATION 7

3.4. FSK/OOK MODE TRANSMITTER SPECIFICATION 8

3.5. DIGITAL SPECIFICATION 8

3.6. ELECTRICAL SPECIFICATION FOR LoRa™ MODULATION 9

4. DP1272 FEATURES 12

4.1. LoRa™ MODEM 12

4.2. FSK/OOK MODEM 12

4.3. RF POWER AMPLIFIERS 12

4.4. HIGH POWER +20 dBm OPERATION 12

5. SPI INTERFACE 13

6. INTRODUCTION TO THE LoRa™ MODEM AND ITS CAPABILITIES 14

7. LINK DESIGN USING THE LoRa™ MODEM 15

7.1. OVERVIEW 15

7.2. LoRa™ PACKET STRUCTURE 16

7.3. PREAMBLE 16

7.4. HEADER 16

7.4.1. Explicit Header Mode 16

7.5. IMPLICIT HEADER MODE 16

7.6. PAYLOAD 16

7.7. TIME ON AIR 17

7.8. FREQUENCY HOPPING WITH LoRa™ 17

7.8.1. PRINCIPLE OF OPERATION 18

7.8.2. TIMING OF CHANNEL UPDATES 18

10. FSK/OOK MODEM 19

10.1. BIT RATE SETTING 19

11. OPERATING MODES IN FSK/OOK MODE 20

11.1. GENERAL OVERVIEW 20

11.2. STARTUP TIMES 20

www.anylink.de
info@anylink.de

11.2.1. TRANSMITTER STARTUP TIME 21
11.2.2. RECEIVER STARTUP TIME 21
11.2.3. TIME TO RSSI EVALUATION 22
11.2.4. TX TO RX TURNAROUND TIME 22
11.2.5. RX TO TX 22
11.2.6. RECEIVER HOPPING; RX TO RX 23
11.2.7. TX TO TX 23
11.3. RECEIVER STARTUP OPTIONS 24
11.4. RECEIVER RESTART METHODS 24
11.4.1. RESTART UPON USER REQUEST 24
11.4.2. AUTOMATIC RESTART AFTER VALID PACKET RECEPTION 24
11.4.3. AUTOMATIC RESTART WHEN PACKET COLLISION IS DETECTED 25
11.5. TOP LEVEL SEQUENCER 25
11.5.1. SEQUENCER STATES 25
11.5.2. SEQUENCER TRANSITIONS 26
11.5.3. TIMERS 27
11.5.4. SEQUENCER STATE MACHINE 28
12. PACKET FORMAT 29
12.1. FIXED LENGTH PACKET FORMAT 29
12.2. VARIABLE LENGTH PACKET FORMAT 29
12.3. UNLIMITED LENGTH PACKET FORMAT 30
13. MECHANICAL DIMENSIONS 31

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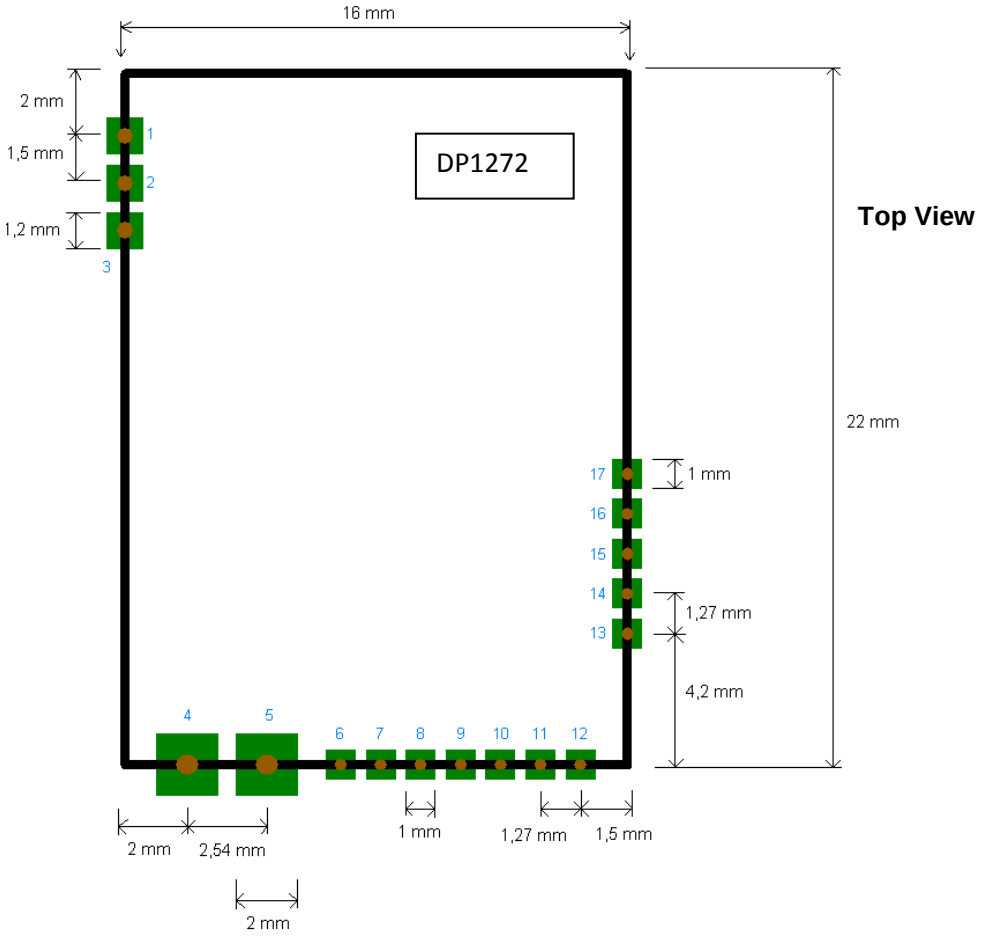
1. PIN DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	GND		Ground.
2	RFIO	IN/OUT	RF input / output
3	GND		Ground.
4	VCC		Supply voltage.
5	GND		Ground.
6	RESET	IN	Reset trigger input.
7	DIO0	IN/OUT	Digital I/O, software configured.
8	DIO1/DCLK	IN/OUT	Digital I/O, software configured.
9	DIO2/DATA	IN/OUT	Digital I/O, software configured.
10	DIO3	IN/OUT	Digital I/O, software configured.
11	DIO4	IN/OUT	Digital I/O, software configured.
12	DIO5	IN/OUT	Digital I/O, software configured.
13	SCK	IN	SPI Clock input.
14	MISO	Out	SPI Data output.
15	MOSI	IN	SPI Data input.
16	NSS	IN	SPI Chip select input.
17	RF_MOD	OUT	RF Mode output, NC if unused.

Table 1

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2. ELECTRICAL CHARACTERISTICS

2.1. Absolute Maximum Ratings

Description	Min	Max	Unit
Supply voltage	0.5	3.9	V
Operating temperature	-55	+115	°C
RF Input Level	-	+10	dBm
Load capacitance on digital ports	-	25	pF

Table 1

2.2. OPERATING RANGE

Description	Min	Max	Unit
Supply voltage	1.8	3.7	V
Operating temperature	-40	+85	°C
Load capacitance on digital ports	-	25	pF
RF Input Level	-	+10	dBm
Soldering temperature (max 15 sec)		260	°C

Table 2

CAUTION: ESD sensitive device.
Precaution should be taken when handling the device in order to prevent permanent damage

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3. SPECIFICATIONS

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1=VBAT2=VDD=3.3 V, temperature = 25 °C, FXOSC = 32 MHz, FRF = 915 MHz, Pout = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified. Shared Rx and Tx path matching.

Note Unless otherwise specified, the performance in the 868 MHz band is identical or better.

3.1. POWER CONSUMPTION SPECIFICATION

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in Sleep mode		-	7	1	µA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	8.5	-	µA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.4	1.6	mA
IDDFS	Supply current in Synthesizer mode	FSRx	-	4.5	-	mA
IDDR	Supply current in Receive mode	LnaBoost = 00	-	10.5	-	mA
IDDT	Supply current in Transmit mode with impedance matching	RFOP = +20 dBm, on PA_BOOST RFOP = +17 dBm, on PA_BOOST	- -	125 90	- -	mA mA

Table 3

3.2. FREQUENCY SYNTHESIZER SPECIFICATION

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range	Programmable	860	-	1020	MHz
FXOSC	Crystal oscillator frequency		-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time		-	250	-	µs
TS_FS	Frequency synthesizer wake-up time to PllLock signal	From Standby mode	-	60	-	µs
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target frequency	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 50 50 50	- - - - - - -	µs µs µs µs µs µs µs
FSTEP	Frequency synthesizer step		-	61.0	-	Hz
FRC	RC Oscillator frequency		-	62.5	-	kHz
BRF	Bit rate, FSK	Programmable values (1)	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps
BRA	Bit Rate Accuracy	ABS(wanted BR - available BR)	-	-	250	ppm
FDA	Frequency deviation, FSK (1)	Programmable FDA + BRF/2 =< 250 kHz	0.6	-	200	kHz

Table 4

Note: For Maximum Bit rate the maximum modulation index is 1.

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3.3. FSK/OOK MODE RECEIVER SPECIFICATION

All receiver tests are performed with RxBw = 10 kHz (Single Side Bandwidth) as programmed in RegRxBw, receiving a PN15 sequence. Sensitivities are reported for a 0.1% BER (with Bit Synchronizer enabled), unless otherwise specified.
Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the receiver sensitivity level.

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	Direct tie of RFI and RFO pins, shared Rx, Tx paths FSK sensitivity, highest LNA gain.	FDA = 5 kHz, BR = 1.2 kb/s	-	-119	-	dBm
		FDA = 5 kHz, BR = 4.8 kb/s	-	-115	-	dBm
		FDA = 40 kHz, BR = 38.4 kb/s*	-	-105	-	dBm
		FDA = 20 kHz, BR = 38.4 kb/s**	-	-106	-	dBm
		FDA = 62.5 kHz, BR = 250 kb/s***	-	-92	-	dBm
	Split RF paths, LnaBoost is turned on, the RF switch insertion loss is not accounted for.	FDA = 5 kHz, BR = 1.2 kb/s	-	-123	-	dBm
		FDA = 5 kHz, BR = 4.8 kb/s	-	-119	-	dBm
		FDA = 40 kHz, BR = 38.4 kb/s*	-	-110	-	dBm
		FDA = 20 kHz, BR = 38.4 kb/s**	-	-110	-	dBm
		FDA = 62.5 kHz, BR = 250 kb/s***	-	-97	-	dBm
RFS_O	OOK sensitivity, highest LNA gain shared Rx, Tx paths	BR = 4.8 kb/s	-	-117	-	dBm
		BR = 32 kb/s	-	-108	-	dBm
CCR	Co-Channel Rejection		-	-9	-	dB
ACR	Adjacent Channel Rejection	FDA = 2 kHz, BR = 1.2kb/s, RxBw = 5.2kHz Offset = +/- 25 kHz	-	54	-	dB
		FDA = 5 kHz, BR=4.8kb/s				
		Offset = +/- 25 kHz	-	50	-	dB
		Offset = +/- 50 kHz	-	50	-	dB
BI	Blocking Immunity	Offset = +/- 1 MHz	-	73	-	dB
		Offset = +/- 2 MHz	-	78	-	dB
		Offset = +/- 10 MHz	-	87	-	dB
AMR	AM Rejection, AM modulated interfere with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz	-	73	-	dB
		Offset = +/- 2 MHz	-	78	-	dB
		Offset = +/- 10 MHz	-	87	-	dB
IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Highest LNA gain	-	+57	-	dBm
IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Highest LNA gain G1	-	-12.5	-	dBm
		LNA gain G2, 4dB sensitivity hit	-	-8	-	dBm
BW_SSB	Single Side channel filter BW	Programmable	2.7	-	250	kHz
IMR	Image Rejection	Wanted signal 3dB over sens BER=0.1%	-	48	-	dB
IMA	Image Attenuation		-	56	-	dB
DR_RSSI	RSSI Dynamic Range	AGC enabled				
		Min	-	-127	-	dBm
		Max	-	0	-	dBm

Table 5

** RxBw = 83 kHz (Single Side Bandwidth)*
*** RxBw = 50 kHz (Single Side Bandwidth)*
**** RxBw = 250 kHz (Single Side Bandwidth)*

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3.4. FSK/OOK MODE TRANSMITTER SPECIFICATION

Symbol	Description	Conditions	Min	Typ	Max	Unit
RF_OP	RF output power in 50 ohms on RFO pin (High efficiency PA).	Programmable with steps Max Min	 +11 -	 +14 -1	 - -	 dBm dBm
ΔRF_ OP_V	RF output power stability on RFO pin versus voltage supply.	VDD = 2.5 V to 3.3 V VDD = 1.8 V to 3.7 V	- -	3 8	- -	dB dB
RF_OPH	RF output power in 50 ohms, on PA_BOOST pin (Regulated PA).	Programmable with 1dB steps Max Min	 - -	 +17 +2	 - -	 dBm dBm
RF_OPH _MAX	Max RF output power, on PA_BOOST pin	High power mode	-	+20	-	dBm
ΔRF_ OPH_V	RF output power stability on PA_BOOST pin versus voltage supply.	VDD = 2.4 V to 3.7 V	-	±1	-	dB
ΔRF_T	RF output power stability versus temperature on both RF pins.	From T = -40 °C to +85 °C	-	+/-1	-	dB
PHN	Transmitter Phase Noise	Low Consumption PLL, 915 MHz 50kHz Offset 400kHz Offset 1MHz Offset	 - - -	 -102 -114 -120	 - - -	dBc/ Hz
		Low Phase Noise PLL, 915 MHz 50kHz Offset 400kHz Offset 1MHz Offset	 - - -	 -106 -117 -122	 - - -	dBc/ Hz
ACP	Transmitter adjacent channel power (measured at 25 kHz offset)	BT=1. Measurement conditions as defined by EN 300 220-1 V2.3.1	-	-	-37	dBm
TS_TR	Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10us, BR = 4.8 kb/s	-	120	-	µs

Table 6

3.5. DIGITAL SPECIFICATION

Conditions: Temp = 25° C, VDD = 3.3 V, FXOSC = 32 MHz, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Digital input level high		0.8	-	-	VDD
VIL	Digital input level low		-	-	0.2	VDD
VOH	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
VOL	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
FSCK	SCK frequency		-	-	10	MHz
tch	SCK high time		50	-	-	ns
tcl	SCK low time		50	-	-	ns
trise	SCK rise time		-	5	-	ns
tfall	SCK fall time		-	5	-	ns
tsetup	MOSI setup time	From MOSI change to SCK rising edge.	30	-	-	ns
thold	MOSI hold time	From SCK rising edge to MOSI change.	20	-	-	ns
tnsetup	NSS setup time	From NSS falling edge to SCK rising edge.	30	-	-	ns
tnhold	NSS hold time	From SCK falling edge to NSS rising edge, normal mode.	100	-	-	ns
tnhigh	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

Table 7

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3.6. ELECTRICAL SPECIFICATION FOR LoRa™ MODULATION

The table below gives the electrical specifications for the transceiver operating with LoRa™ modulation. Following conditions apply unless otherwise specified:

- Supply voltage = 3.3 V.
- Temperature = 25° C.
- fXOSC = 32 MHz.
- Band: fRF = 915 MHz.
- bandwidth (BW) = 125 kHz.
- Spreading Factor (SF) = 12.
- Error Correction Code (EC) = 4/6.
- Packet Error Rate (PER)= 1%.
- CRC on payload enabled.
- Output power = 13 dBm in transmission.
- Payload length = 12 symbols (programmed register PreambleLength=8)
- With matched impedances.

Electrical specifications: LoRa™ mode

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDR_L	Supply current in receiver LoRa™ mode, 868 MHz	LnaBoost Off, BW = 125 kHz	-	9,7	-	mA
		LnaBoost Off, BW = 250 kHz	-	10,5	-	mA
		LnaBoost Off, BW = 500 kHz	-	12	-	mA
		LnaBoost On, BW = 125 kHz	-	10,8	-	mA
		LnaBoost On, BW = 250 kHz	-	11,6	-	mA
		LnaBoost On, BW = 500 kHz	-	13	-	mA
IDDT_L	Supply current in transmitter mode	RFOP = 13 dBm	-	32	-	mA
		RFOP = 7 dBm	-	22	-	mA
IDDT_H_L	Supply current in transmitter mode with an external impedance transformation	Using PA_BOOST pin RFOP = 17 dBm	-	92	-	mA
BI_L	Blocking immunity, FRF=868 MHz CW interferer	offset = +/- 1 MHz	-	82.5	-	dB
		offset = +/- 2 MHz	-	86.5	-	dB
		offset = +/- 10 MHz	-	89	-	dB
IIP3_L	3rd order input intercept point, highest LNA gain, FRF=868 MHz, CW interferer	F1 = FRF + 1 MHz F2 = FRF + 1.995 MHz	-	*-12.5*	-	*dBm*
IIP2_L	2nd order input intercept point, highest LNA gain, FRF=868 MHz, CW interferer.	F1 = FRF + 20 MHz F2 = FRF+ 20 MHz + Δf	-	*57*	-	*dBm*
BR_L	Bit rate, Long-Range Mode	From SF6, CR = 4/5, BW = 500 kHz to SF12, CR = 4/8, BW = 125 kHz	*0.24*	-	*37.5*	*kbps*
BR_L125	RF sensitivity, Long-Range Mode, highest LNA gain, LNA boost, 125 kHz bandwidth using split Rx/Tx path	SF = 6	-	*-121*	-	*dBm*
		SF = 7	-	*-124*	-	*dBm*
		SF = 8	-	*-127*	-	*dBm*
		SF = 9	-	*-130*	-	*dBm*
		SF = 10	-	*-133*	-	*dBm*
		SF = 11	-	*-135*	-	*dBm*
		SF = 12	-	*-137*	-	*dBm*
BR_L250	RF sensitivity, Long-Range Mode, highest LNA gain, LNA boost, 250 kHz bandwidth using split Rx/Tx path	SF = 6	-	*-118*	-	*dBm*
		SF = 7	-	*-122*	-	*dBm*
		SF = 8	-	*-125*	-	*dBm*
		SF = 9	-	*-128*	-	*dBm*
		SF = 10	-	*-130*	-	*dBm*
		SF = 11	-	*-132*	-	*dBm*
		SF = 12	-	*-135*	-	*dBm*
BR_L500	RF sensitivity, Long-Range Mode, highest LNA gain, LNA boost, 500 kHz bandwidth using split Rx/Tx path	SF = 6	-	-111	-	*dBm*
		SF = 7	-	-116	-	*dBm*
		SF = 8	-	-119	-	*dBm*
		SF = 9	-	-122	-	*dBm*

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		SF = 10 SF = 11 SF = 12	- - -	-125 -128 -129	- - -	*dBm* *dBm* *dBm*
CCR_LL	*Co-channel rejection*					
ACR_LCW	*Adjacent channel rejection* *FRF = 868 MHz*					
IMR_LCW	*Image rejection after calibration*					
FERR_L	*Maximum tolerated frequency offset between transmitter and receiver, no sensitivity degradation*					

Table 8

Electrical specifications: LoRa™ mode

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_L125	RF sensitivity, Long-Range Mode, highest LNA gain, LNA boost, 125 kHz bandwidth 1% PER **using individual Rx/Tx path** FRF=868 MHz, 10 byte	CR = 4/5, SF = 7 CR = 4/5, SF = 8 CR = 4/5, SF = 9 CR = 4/5, SF = 10 CR = 4/5, SF = 11 CR = 4/5, SF = 12	- - - - - -	-124 -125 -129 -132 -134 -136	- - - - - -	dBm dBm dBm dBm dBm dBm
RFS_L250	RF sensitivity, Long-Range Mode, highest LNA gain, LNA boost, 250 kHz bandwidth 1% PER **using individual Rx/Tx path** FRF=868 MHz, 10 byte	CR = 4/5, SF = 7 CR = 4/5, SF = 8 CR = 4/5, SF = 9 CR = 4/5, SF = 10 CR = 4/5, SF = 11 CR = 4/5, SF = 12	- - - - - -	-120 -122 -125 -129 -131 -133	- - - - - -	dBm dBm dBm dBm dBm dBm
RFS_L500	RF sensitivity, Long-Range Mode, highest LNA gain, LNA boost, 500 kHz bandwidth 1% PER **using individual Rx/Tx path** FRF=868 MHz, 10 byte	CR = 4/5, SF = 7 CR = 4/5, SF = 8 CR = 4/5, SF = 9 CR = 4/5, SF = 10 CR = 4/5, SF = 11 CR = 4/5, SF = 12	- - - - - -	-117 -121 TBC -126 -128 -130	- - - - - -	dBm dBm dBm dBm dBm dBm
CCR_LCW6	Co-channel rejection Single CW tone = Sens +6 dB 1% PER	SF = 12	-	*TBC*	-	*dB*
CCR_LCW	Co-channel rejection Single CW tone = Sens +3 dB 1% PER	SF = 7 SF = 8 SF = 9 SF = 10 SF = 11 SF = 12	-	5 10 12 14 15 18	-	dB dB dB dB dB dB
CCR_LL	Co-channel rejection	Interferer is a LoRa™ signal using same BW and same SF. Pw = Sensitivity + 3 dB		-6		dB
ACR_LCW	Adjacent channel rejection FRF=868MHz	Interferer is 1.5*BW_L from the wanted signal center frequency 1% PER, Single CW tone = Sens + 3 dB SF = 7 SF = 12	 - -	 60 72	 - -	 dB dB
IMR_LCW	Image rejection after calibration.	1% PER, Single CW tone = Sens +3 dB	-	66	-	dB
FERR_L	Maximum tolerated frequency offset between transmitter and receiver	BW_L = 125 kHz BW_L = 250 kHz BW_L = 500 kHz no sensitivity degradation	-30 -60 - 120	- - - -	30 60 120	kHz kHz kHz

Table 9

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4. DP1272 FEATURES

The DP1272 is equipped with both standard FSK and long range spread spectrum (LoRa™) modems. Depending upon the mode selected either conventional OOK or FSK modulation may be employed or the LoRa™ spread spectrum modem.

4.1. LoRa™ MODEM

The LoRa™ modem uses a proprietary spread spectrum modulation technique. This modulation, in contrast to legacy modulation techniques, permits an increase in link budget and increased immunity to in-band interference. At the same time the frequency tolerance requirement of the crystal reference oscillator is relaxed - allowing a performance increase for a reduction in system cost.

4.2. FSK/OOK MODEM

In FSK/OOK mode the DP1272 can avail of standard modulation techniques including OOK, FSK, GFSK, MSK and GMSK. The DP1272 is especially suited to narrow band communication thanks the low-IF architecture employed and the built-in AFC functionality.

4.3. RF POWER AMPLIFIERS

PA1 and PA2 are both connected to pin PA_BOOST. There are two potential configurations of these power Amplifiers, fixed or programmable. In the fixed configuration they can deliver up to +20 dBm. In programmable Configuration they can provide from +17 dBm to +2 dBm in 1 dB programmable steps.

PaSelect	Mode	Power Range	Pout Formula
0	PA1 and PA2 combined on pin PA_BOOST	+2 to +17 dBm	+2 dBm + *OutputPower*
1	PA1+PA2 on PA_BOOST with high output power +20 dBm	+5 to +20 dBm	+5 dBm + *OutputPower*

Table 10 Power Amplifier Mode Selection Truth Table

Note:

- For +20 dBm restrictions on operation please consult the following section.
- To ensure correct operation at the highest power levels ensure that the current limiter OcpTrim is adjusted to permit delivery of the requisite supply current.

4.4. HIGH POWER +20 dBm OPERATION

The DP1272 has a high power +20 dBm capability on PA_BOOST pin, with the following settings:

Register	Address	Value for High Power	Default value PA0 or +17dBm	Description
RegPaDac	0x5A	0x87	0x84	High power PA control

Table 11 High Power Settings

Note:

- High Power settings must be turned off when using PA0
- The Over Current Protection limit should be adapted to the actual power level, in RegOcp

Specific Absolute Maximum Ratings and Operating Range restrictions apply to the +20 dBm operation. They are listed in Table 12 and Table 13.

Symbol	Description	Min	Max	Unit
DC_20dBm	Duty Cycle of transmission at +20 dBm output	-	1	%
VSWR_20dBm	Maximum VSWR at antenna port, +20 dBm output	-	3:1	-

Table 12 Operating Range, +20dBm Operation

Symbol	Description	Min	Max	Unit
VDDop_20dBm	Supply voltage, +20 dBm output	2.4	3.7	V

Table 13 Operating Range, +20dBm Operation

The duty cycle of transmission at +20 dBm is limited to 1%, with a maximum VSWR of 3:1 at antenna port, over the Standard operating range [-40;+85°C]. For any other operating condition, contact your Anylink representative.

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5. SPI INTERFACE

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

- SINGLE access: an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the beginning of the frame and goes high after the data byte.
- BURST access: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. These modes are available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.
- FIFO access: if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

The figure below shows a typical SPI single access to a register.

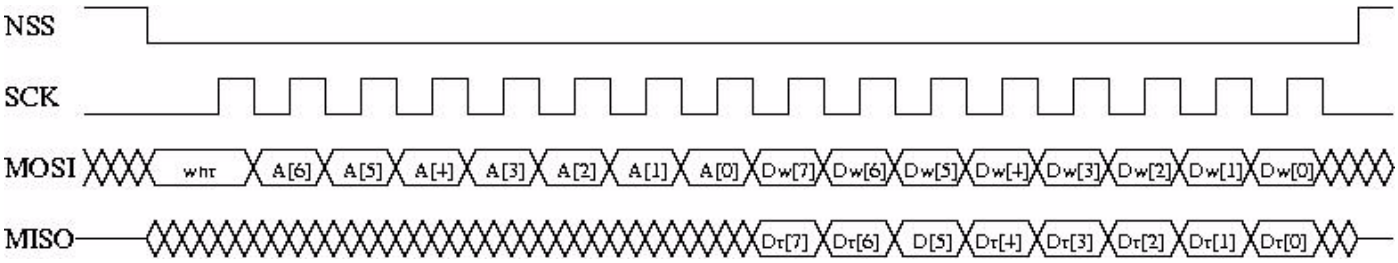

Figure 1 SPI Timing Diagram (single access)

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.
A transfer is always started by the NSS pin going low. MISO is high impedance when NSS is high.

The first byte is the address byte. It is comprises:

- A wnr bit, which is 1 for write access and 0 for read access.
- Then 7 bits of address, MSB first.

The second byte is a data byte, either sent on MOSI by the master in case of a write access or received by the master on MISO in case of read access. The data byte is transmitted MSB first.

Proceeding bytes may be sent on MOSI (for write access) or received on MISO (for read access) without a rising NSS edge and re-sending the address. In FIFO mode, if the address was the FIFO address then the bytes will be written / read at the FIFO address. In Burst mode, if the address was not the FIFO address, then it is automatically incremented for each new byte received.

The frame ends when NSS goes high. The next frame must start with an address byte. The SINGLE access mode is therefore a special case of FIFO / BURST mode with only 1 data byte transferred.

During the write access, the byte transferred from the slave to the master on the MISO line is the value of the written register before the write operation.

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6. INTRODUCTION TO THE LoRa™ MODEM AND ITS CAPABILITIES

The LoRa™ modem uses spread spectrum modulation and forward error correction techniques to increase the range and robustness of radio communication links compared to traditional FSK or OOK based modulation. Examples of the performance improvement possible, for several possible settings, are summarized in the table below. Here the spreading factor and error correction rate are design variables that allow the designer to optimize the trade-off between occupied bandwidth, data rate, link budget improvement and immunity to interference.

Bandwidth (kHz)	Spreading Factor	Coding rate	Nominal Rb (bps)	Sensitivity (dBm)	SNR Min (dB)
125	7	4/5	5469	-124	TBC
125	12	4/5	293	-136	TBC
250	7	4/5	10938	-120	TBC
250	12	4/5	586	-133	TBC
500	7	4/5	21875	-117	TBC
500	12	4/5	1172	-130	TBC

Table 14 Example LoRa™ Modem Performances

Typically such performance gains require high stability frequency references, with LoRa™ this is not the case. The figure below shows the link budget improvement as a function of the frequency offset between LoRa™ transmitter and receiver.

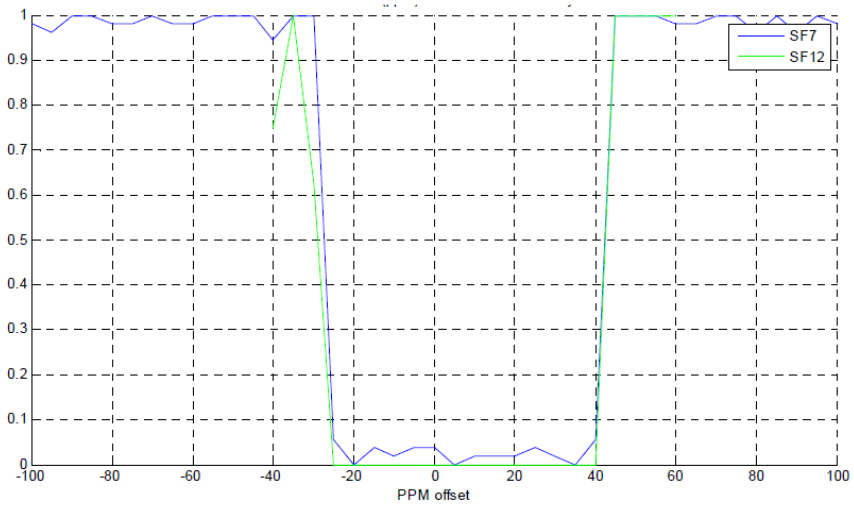

Figure 2 Influence of Frequency Drift on LoRa™ Modem Sensitivity (SF = 7, BW = 500 kHz & f = 915 MHz)

For European operation the range of crystal tolerances acceptable for each sub-band (of the ERC 70-03) is given in the specifications table. For US based operation a frequency hopping mode is available that automates both the LoRa™ spread spectrum and frequency hopping spread spectrum processes.

Another important facet of the LoRa™ modem is its increased immunity to interference. The LoRa™ modem is capable of co-channel GMSK rejection of up to 25 dB. This immunity to interference permits the simple coexistence of LoRa™ modulated systems either in bands of heavy spectral usage or in hybrid communication networks that use LoRa™ to extend range when legacy modulation schemes fail.

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7. LINK DESIGN USING THE LoRa™ MODEM

7.1. OVERVIEW

The LoRa™ modem is setup as shown in the following figure. This configuration permits the simple replacement of the FSK modem with the LoRa™ modem via the configuration register setting RegOpMode. This change can be performed on the fly (in Sleep operating mode) thus permitting the use of both standard FSK or OOK in conjunction with the long range capability. The LoRa™ modulation and demodulation process is proprietary, it uses a form of spread spectrum modulation combined with cyclic error correction coding. The combined influence of these two factors is an increase in link budget and enhanced immunity to interference.

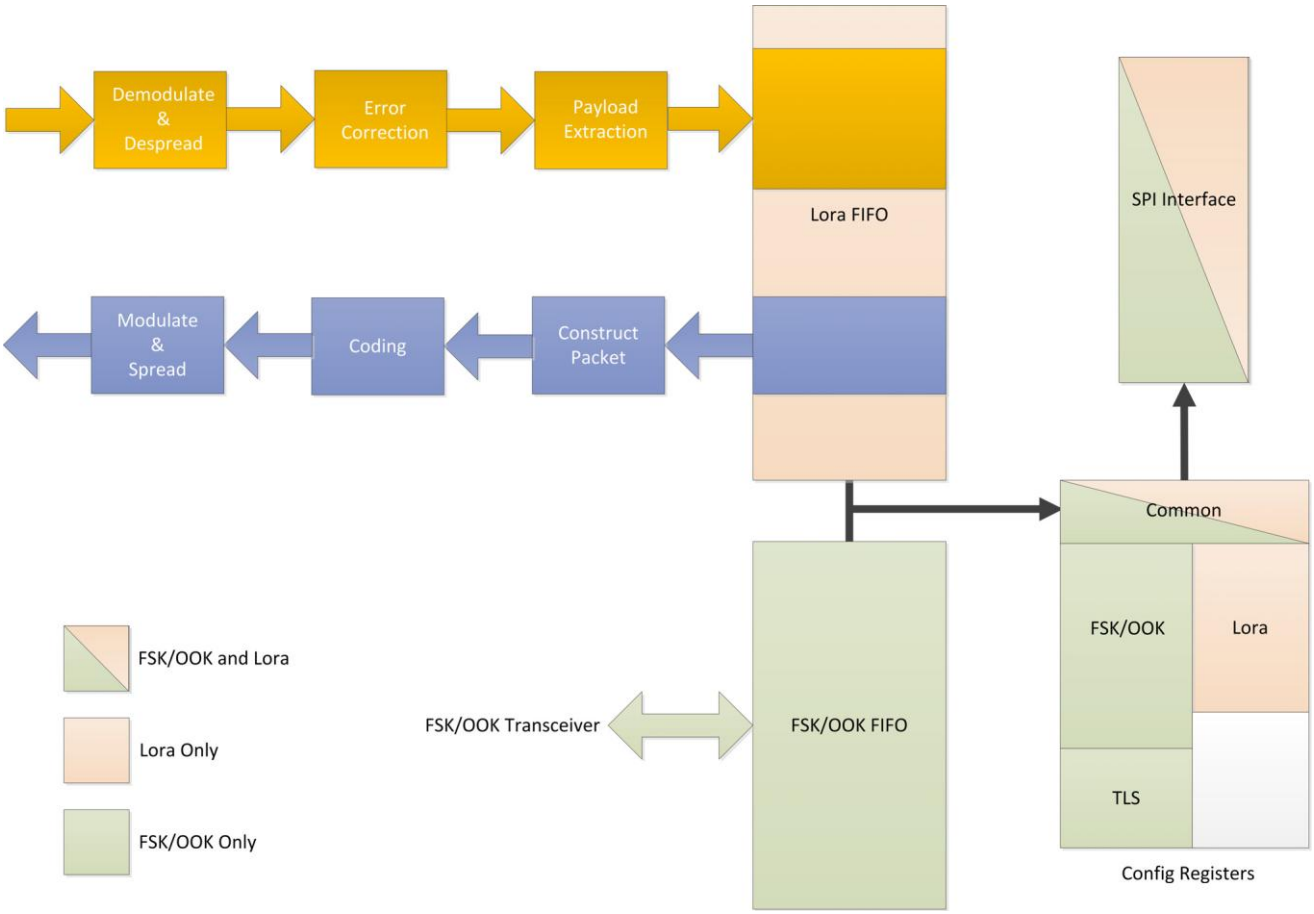


Figure 3 LoRa™ Modem Connectivity

A simplified outline of the transmit and receive processes is also shown above. Here we see that the LoRa™ modem has an independent dual port data buffer FIFO that is accessed through the SPI interface common to all modes. Upon selection of LoRa™ mode, the configuration register mapping of the DP1272 changes. For full details of this change please consult the register description of Semtech SX1272 Datasheet. (www.semtech.com)

So that it is possible to optimize the LoRa™ modulation for a given application, access is given to the designer to three critical design parameters. Each one permitting a tradeoff between link budget, immunity to interference, spectral occupancy and nominal data rate. These parameters are spreading factor, modulation bandwidth and error coding rate.

7.2. LoRa™ PACKET STRUCTURE

The LoRa™ modem employs two types of packet format, explicit and implicit. The explicit packet includes a short header that contains information about the number of bytes, coding rate and whether a CRC is used in the packet. The packet format is shown in the following figure.

The LoRa™ packet comprises three elements:

- A preamble.
- An optional header.
- The data payload.

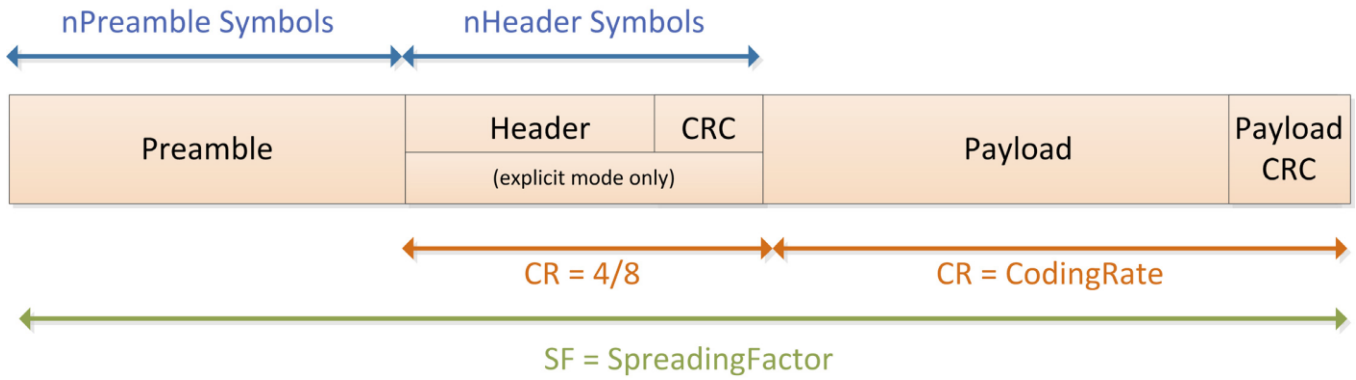


Figure 4 LoRa™ Packet Structure

7.3. PREAMBLE

The preamble is used to synchronize receiver with the incoming data flow. Although by default, it consists of a 12 symbol long sequence - the receiver does not require knowledge of the preamble length. The preamble length may be extended in the interest of reducing to receiver duty cycle in receive intensive applications. However, the minimum length suffices for all communication. The transmitted preamble length may be changed by setting the register PreambleLength from 12 to 32768.

7.4. HEADER

Depending upon the chosen mode of operation two types of header are available. The header type is selected by the ImplictHeaderMode bit found within the RegSymbTimeoutMsb register.

7.4.1. Explicit Header Mode

This is the default mode of operation. Here the header provides information on the payload, namely:

- The payload length in bytes.
- The forward error correction code rate
- The presence of an optional 16-bits CRC for the payload.

The header is transmitted with maximum error correction code (4/8). It also has its own CRC to allow the receiver to discard invalid headers.

7.5. IMPLICIT HEADER MODE

In certain scenarios, where the payload, coding rate and CRC presence are fixed or known in advance, it may be advantageous to reduce transmission time by invoking implicit header mode. In this mode the header is removed from the packet. In this case the payload length, error coding rate and presence of the payload CRC must be manually configured on both sides of the radio link.

7.6. PAYLOAD

The packet payload is a variable-length field that contains the actual data coded at the error rate either as specified in the header in explicit mode or in the register settings in implicit mode. An optional CRC may be appended.

7.7. TIME ON AIR

For a given combination of spreading factor (SF), coding rate (CR) and signal bandwidth (BW) the total on-the-air transmission time of a LoRa™ packet can be calculated as follows:

With standard header:

$$TotalTimeOnAir = \frac{Nb_{symbol_{header_{wpayload}}} * 2^{SF}}{BW}$$

$$Nb_{symbol_{header_{wpayload}}} = Nb_{symbol_{payload}} + PREAMB\_SYMB + 4.25 + 8$$

PREAMB_SYMB is the number of programmed preamble symbols.

$$Nb_{symbol_{payload}} = CEIL(Nb\_symbol\_payload\_frac, 4 + CR)$$

CEIL is the function that rounds to the integer multiple of 4+CR immediately superior to the fractional first parameter.

$$Nb_{symbol_{payload_{frac}}} = \frac{a(PL \times 8 + 16 \times CRC(-4 \times (SF - 7))) \times (4 + CR))}{b(4 \times SF)}$$

- CRC = 0 or 1, 16 bits payload checksum enabled (1) or not (0)
- CR = 0 or 4: coding rate of the payload with ratio = 4/(4+CR). CR=4 =max coding redundancy, CR = 0 means no error correction.
- PL = 1 to 255, number of bytes of the payload (user data)

In implicit header mode the formulae are identical bar Nb_symbol_payload_frac which becomes:

$$Nb_{symbol_{payload_{frac}}} = \frac{(PL \times 8 + 16 \bullet CRC - 4 \times (SF - 2)) \times (4 + CR)}{(4 \times SF)}$$

7.8. FREQUENCY HOPPING WITH LoRa™

The duration of a single packet could exceed regulatory requirements relating to the maximum permittable channel dwell time. To ease implementation and ensure continued compliance when operating in frequency hopping spread spectrum (FHSS) mode (FhssMode of register RegTxCfg1) can be enabled.

7.8.1. PRINCIPLE OF OPERATION

The principle behind the FHSS scheme is that a portion of each LoRa™ packet is transmitted on each hopping channel from a look up table of frequencies managed by the host microcontroller. After a predetermined hopping period the transmitter changes to the next channel in a predefined list of hopping frequencies and continues transmitting the next symbol of the packet. The time which the transmission will last in any given channel is determined by HoppingPeriod which is an integer multiple of symbol periods:

$$HoppingPeriod = Ts \times FreqHoppingPeriod$$

$$Ts = \frac{1}{Rs}$$

The frequency hopping transmission and reception process starts at channel 0, following each frequency hop the channel counter stored in FhssPresentChannel is incremented and the interrupt signal FhssChangeChannel is generated. Upon completion of the transmission on any given channel the companion microcontroller must hence read the FhssPresentChannel value and load the corresponding RF centre frequency into the Frf register.

FHSS Reception always starts on channel 0. The receiver waits for a valid preamble detection before starting the frequency hopping process as described above. Note that in the eventuality of header CRC corruption, the receiver will automatically request channel 0 and recommence the valid preamble detection process.

7.8.2. TIMING OF CHANNEL UPDATES

The interrupt requesting the channel change, FhssChannelChange, is generated at least 1 ms before the next frequency value must be written - allowing ample time for most MCUs to update the register. The frequency hopping process is recapitulated in the diagram below:

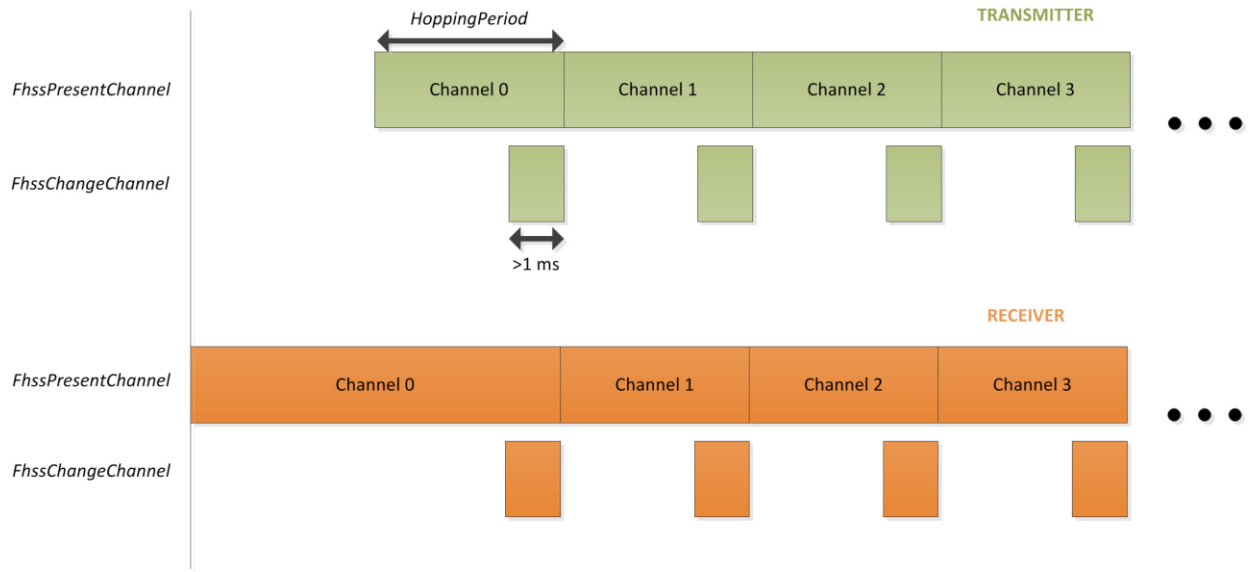


Figure 5 Interrupts generated in the case of successful frequency hopping communication

10. FSK/OOK MODEM

10.1. BIT RATE SETTING

The bitrate setting is referenced to the crystal oscillator and provides a precise means of setting the bit rate (or equivalently chip) rate of the radio. In continuous transmit mode the data stream to be transmitted can be input directly to the modulator via pin 9 (DIO2/DATA) in an asynchronous manner, unless Gaussian filtering is used, in which case the DCLK signal on pin 8 (DIO1/DCLK) is used to synchronize the data stream.

In Packet mode or in Continuous mode with Gaussian filtering enabled, the Bit Rate (BR) is controlled by bits Bitrate in RegBitrateMsb and RegBitrateLsb

$$BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$$

Note: BitrateFrac bits have no effect (i.e may be considered equal to 0) in OOK modulation mode.

The quantity BitrateFrac is hence designed to allow very high precision (max. 250 ppm programing resolution) for any bitrate in the programmable range. Table 24 below shows a range of standard bitrates and the accuracy to within which they may be reached.

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical modem baud rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps		38415.36
	0x01	0xA1	76.8 kbps		76738.60
	0x00	0xD0	153.6 kbps		153846.1
Classical modem baud rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps		57553.95
	0x01	0x16	115.2 kbps		115107.9
Round bit rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x80	0x00	50 kbps		50000.00
	0x01	0x40	100 kbps		100000.0
	0x00	0xD5	150 kbps		150234.7
	0x00	0xA0	200 kbps		200000.0
	0x00	0x80	250 kbps		250000.0
	0x00	0x6B	300 kbps		299065.4
Watch Xtal frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

Table 15 Bit Rate Examples

11. OPERATING MODES IN FSK/OOK MODE

11.1. GENERAL OVERVIEW

The DP1272 has several working modes, manually programmed in RegOpMode. Fully automated mode selection, packet transmission and reception is also possible using the Top Level Sequencer described in Section 11.5.

Mode	Selected mode	Symbol	Enabled blocks
000	Sleep mode	Sleep	None
001	Standby mode	Stdby	Top regulator and crystal oscillator
010	Frequency synthesiser to Tx frequency	FSTx	Frequency synthesizer at Tx frequency (Frf)
011	Transmit mode	Tx	Frequency synthesizer and transmitter
100	Frequency synthesiser to Rx frequency	FSRx	Frequency synthesizer at frequency for reception (Frf-IF)
101	Receive mode	Rx	Frequency synthesizer and receiver

Table 16 Basic Transceiver Modes

When switching from a mode to another the sub-blocks are woken up according to a pre-defined optimized sequence.

11.2. STARTUP TIMES

The startup time of the transmitter or the receiver is dependent upon which mode the transceiver was in at the beginning.
For a complete description, Figure 6 below shows a complete startup process, from the lower power mode “Sleep”.

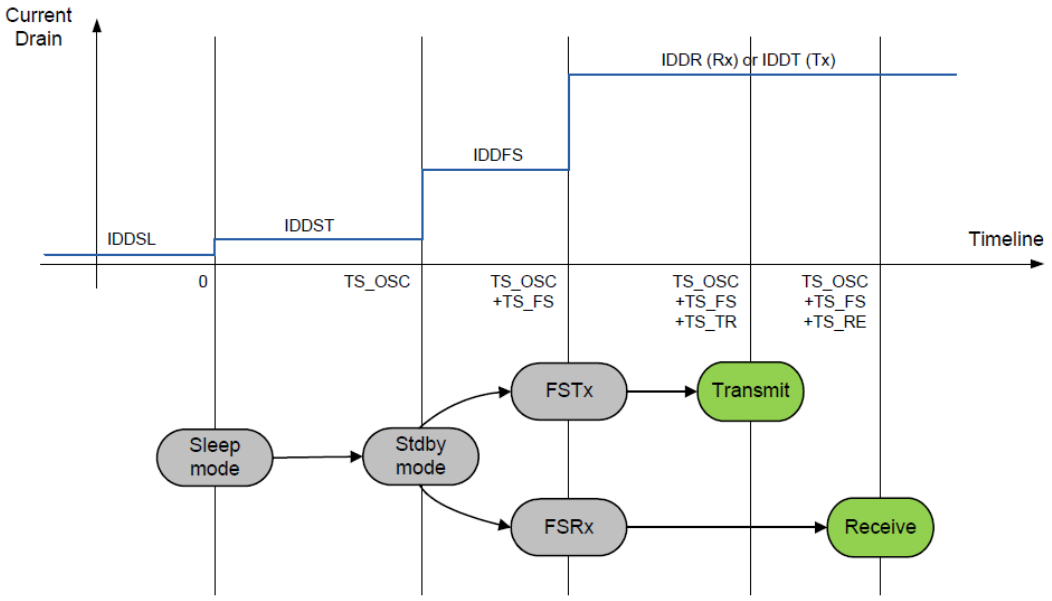


Figure 6 Startup Process

TS_OSC is the startup time of the crystal oscillator which depends on the electrical characteristics of the crystal.
TS_FS is the startup time of the PLL including systematic calibration of the VCO.

11.2.1. TRANSMITTER STARTUP TIME

The transmitter startup time, TS_TR, is calculated as follows in FSK mode:

$$TS\ TR = 5\mu s + 1.25 * PaRamp + \frac{1}{2} * Tbit$$

- PaRamp is the ramp-up time programmed in RegPaRamp.
- Tbit is the bit time.

In OOK mode, this equation can be simplified to the following:

$$TS_{TR} = 5\mu s + \frac{1}{2} * Tbit$$

11.2.2. RECEIVER STARTUP TIME

The receiver startup time, TS_RE, only depends upon the receiver bandwidth effective at the time of startup. When AFC is enabled (AfcAutoOn=1), AfcBw should be used instead of RxBw to extract the receiver startup time:

RxBw if AfcAutoOn=0 RxBwAfc if AfcAutoOn=1	TS_RE (+/-5%)
2.6 kHz	2.33 ms
3.1 kHz	1.94 ms
3.9 kHz	1.56 ms
5.2 kHz	1.18 ms
6.3 kHz	984 µs
7.8 kHz	791 µs
10.4 kHz	601 µs
12.5 kHz	504 µs
15.6 kHz	407 µs
20.8 kHz	313 µs
25.0 kHz	264 µs
31.3 kHz	215 µs
41.7 kHz	169 µs
50.0 kHz	144 µs
62.5 kHz	119 µs
83.3 kHz	97 µs
100.0 kHz	84 µs
125.0 kHz	71 µs
166.7 kHz	85 µs
200.0 kHz	74 µs
250.0 kHz	63 µs

Table 17 Receiver Startup Time Summary

TS_RE or later after setting the device in Receive mode, any incoming packet will be detected and demodulated by the transceiver.

11.2.3. TIME TO RSSI EVALUATION

The first RSSI sample will be available TS_RSSI after the receiver is ready, in other words TS_RE + TS_RSSI after the receiver was requested to turn on.

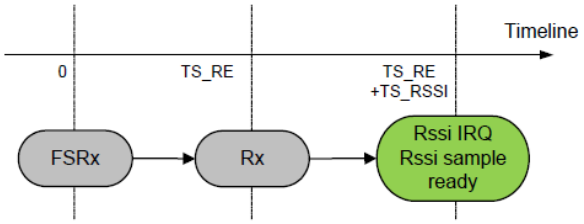


Figure 7 Time to Rssi Sample

TS_RSSI depends on the receiver bandwidth, as well as the *RssiSmoothing* option that was selected.

11.2.4. TX TO RX TURNAROUND TIME

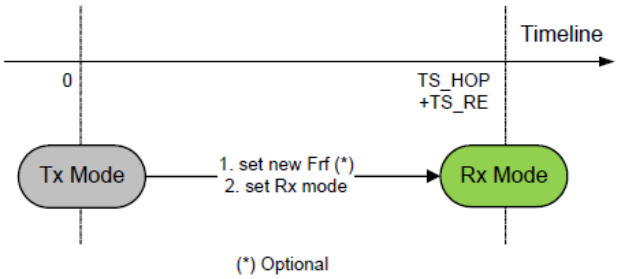


Figure 8 Tx to Rx Turnaround

Note The SPI instruction times are omitted, as they can generally be very small as compared to other timings (up to 10MHz SPI clock).

11.2.5. RX TO TX

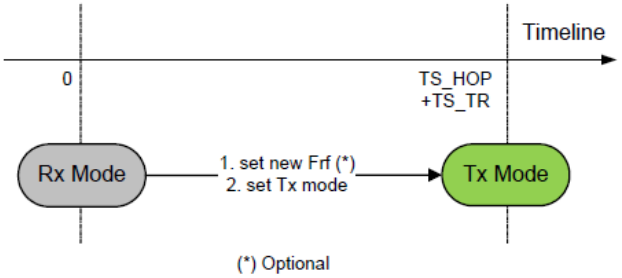


Figure 9 Rx to Tx Turnaround

11.2.6. RECEIVER HOPPING; RX TO RX

Two methods are possible:

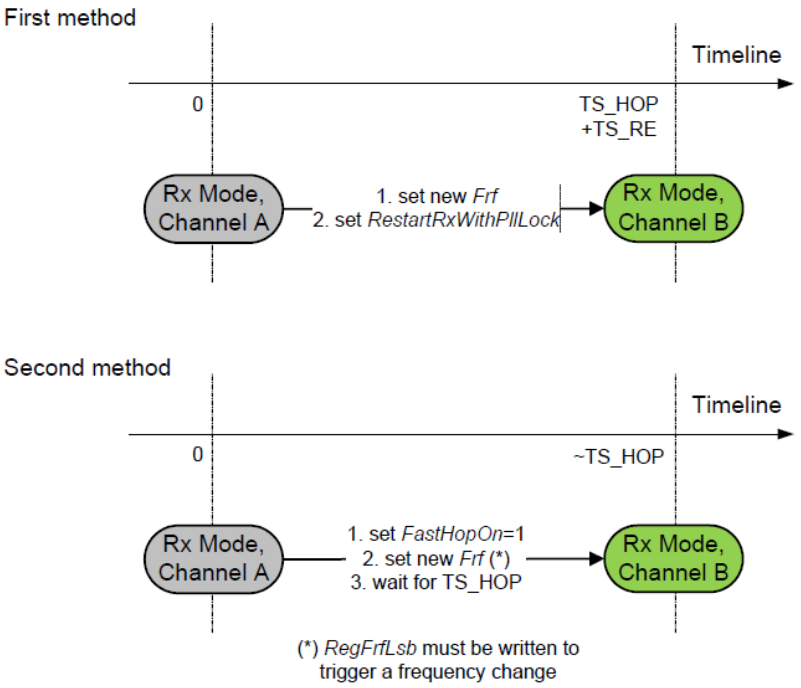


Figure 10 Receiver Hopping

The second method is quicker, and should be used if a very quick RF sniffing mechanism is to be implemented.

11.2.7. TX TO TX

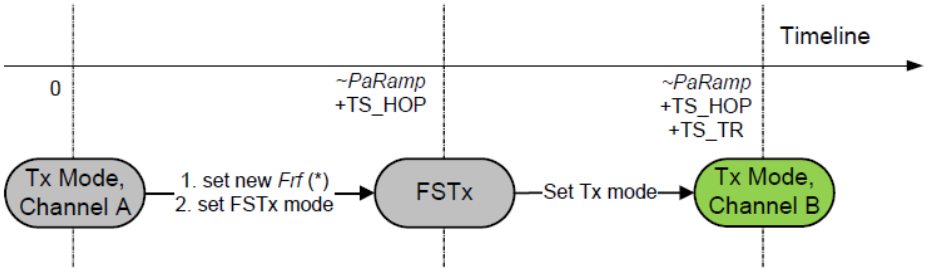


Figure 11 Transmitter Hopping

11.3. RECEIVER STARTUP OPTIONS

The DP1272 receiver can automatically control the gain of the receive chain (AGC) and adjust the receiver LO frequency (AFC). Those processes are carried out on a packet-by-packet basis. They occur:

- When the receiver is turned On.
- When the Receiver is restarted upon user request, through the use of trigger bits RestartRxWithoutPllLock or RestartRxWithPllLock, in RegRxConfig.
- When the receiver is automatically restarted after the reception of a valid packet, or after a packet collision.

The receiver startup options available in DP1272 are described in Table 18.

Triggering Event	Realized Function	AgcAutoOn	AfcAutoOn	RxTrigger (2:0)
None	None	0	0	000
Rssi Interrupt	AGC	1	0	001
	AGC & AFC	1	1	001
PreambleDetect	AGC	1	0	110
	AGC & AFC	1	1	110
Rssi Interrupt & *PreambleDetect*	AGC	1	0	111
	AGC & AFC	1	1	111

Table 18 Receiver Startup Options

When *AgcAutoOn*=0, the LNA gain is manually selected by choosing *LnaGain* bits in *RegLna.*

11.4. RECEIVER RESTART METHODS

The options for restart of the receiver are covered below. This is typically of use to prepare for the reception of a new signal whose strength or carrier frequency is different from the preceding packet to allow the AGC or AFC to be re-evaluated.

11.4.1. RESTART UPON USER REQUEST

In Receive mode the user can request a receiver restart - this can be useful in conjunction with the use of a Timeout interrupt following a period of inactivity in the channel of interest. Two options are available:

- No change in the Local Oscillator upon restart: the AFC is disabled, and the Frf register has not been changed through SPI before the restart instruction: set bit RestartRxWithoutPllLock in RegRxConfig to 1.
- Local Oscillator change upon restart: if AFC is enabled (AfcAutoOn=1), and/or the Frf register had been changed during the last Rx period: set bit RestartRxWithPllLock in RegRxConfig to 1.

Note ModeReady must be at logic level 1 for a new RestartRx command to be taken into account.

11.4.2. AUTOMATIC RESTART AFTER VALID PACKET RECEPTION

The bits AutoRestartRxMode in RegSyncConfig control the automatic restart feature of the DP1272 receiver, when a valid packet has been received:

- If AutoRestartRxMode = 00, the function is off, and the user should manually restart the receiver upon valid packet reception.
- If AutoRestartRxMode = 01, after the user has emptied the FIFO following a PayloadReady interrupt, the receiver will automatically restart itself after a delay of InterPacketRxDelay, allowing for the distant transmitter to ramp down, hence avoiding a false RSSI detection on the ‘tail’ of the previous packet.
- If AutoRestartRxMode = 10 should be used if the next reception is expected on a new frequency, i.e. Frf is changed after the reception of the previous packet. An additional delay is systematically added, in order for the PLL to lock at a new frequency.

11.4.3. AUTOMATIC RESTART WHEN PACKET COLLISION IS DETECTED

In receive mode the DP1272 is able to detect packet collision and restart the receiver. Collisions are detected by a sudden rise in received signal strength, detected by the RSSI. This functionality can be useful in network configurations where many asynchronous slaves attempt periodic communication with a single a master node.

The collision detector is enabled by setting bit RestartRxOnCollision to 1.

The decision to restart the receiver is based on the detection of RSSI change. The sensitivity of the system can be adjusted in 1 dB steps by using register RssiCollisionThreshold in RegRxConfig.

11.5. TOP LEVEL SEQUENCER

Depending on the application, it is desirable to be able to change the mode of the circuit according to a predefined sequence without access to the serial interface. In order to define different sequences or scenarios, a user-programmable state machine, called Top Level Sequencer (Sequencer in short), can automatically control the chip modes.

NOTE: ***THIS FUNCTIONALITY IS ONLY AVAILABLE IN FSK/OOK MODE.***

The Sequencer is activated by setting the SequencerStart bit in RegSeqConfig1 to 1 in Sleep or Standby mode (called initial mode).

It is also possible to force the Sequencer off by setting the Stop bit in RegSeqConfig1 to 1 at any time.

Note SequencerStart and Stop bit must never be set at the same time.

11.5.1. SEQUENCER STATES

As shown in the table below, with the aid of a pair of interrupt timers (T1 and T2), the sequencer can take control of the chip operation in all modes.

Sequencer State	Description
SequencerOff State	The Sequencer is not activated. Sending a *SequencerStart* command will launch it. When coming from **LowPowerSelection** state, the Sequencer will be Off, whilst the chip will return to its initial mode (either Sleep or Standby mode).
Idle State	The chip is in low-power mode, either *Standby* or *Sleep*, as defined by *IdleMode* in *RegSeqConfig1*. The Sequencer waits only for the *T1* interrupt.
Transmit State	The transmitter in on.
Receive State	The receiver in on.
PacketReceived	The receiver is on and a packet has been received. It is stored in the FIFO.
LowPowerSelection	Selects low power state (**SequencerOff** or **Idle** State)
RxTimeout	Defines the action to be taken on a RxTimeout interrupt. RxTimeout interrupt can be a *TimeoutRxRssi*, *TimeoutRxPreamble* or *TimeoutSignalSync* interrupt.

Table 19 Sequencer States

11.5.2. SEQUENCER TRANSITIONS

The transitions between sequencer states are listed in the forthcoming table.

Variable	Transition
IdleMode	Selects the chip mode during **Idle** state: 0: *Standby* mode 1: *Sleep* mode
FromStart	Controls the Sequencer transition when the *SequencerStart* bit is set to 1 in *Sleep* or *Standby* mode: 00: to **LowPowerSelection** 01: to **Receive** state 10: to **Transmit** state 11: to **Transmit** state on a *FifoThreshold* interrupt
LowPowerSelection	Selects Sequencer LowPower state after a *to LowPowerSelection* transition 0: **SequencerOff** state with chip on Initial mode 1: **Idle** state with chip on *Standby* or *Sleep* mode depending on **IdleMode** Note: Initial mode is the chip LowPower mode at Sequencer start.
FromIdle	Controls the Sequencer transition from the **Idle** state on a *T1* interrupt: 0: to **Transmit** state 1: to **Receive** state
FromTransmit	Controls the Sequencer transition from the **Transmit** state: 0: to **LowPowerSelection** on a *PacketSent* interrupt 1: to **Receive** state on a *PacketSent* interrupt
FromReceive	Controls the Sequencer transition from the **Receive** state: 000 and 111: unused 001: to **PacketReceived** state on a *PayloadReady* interrupt 010: to **LowPowerSelection** on a *PayloadReady* interrupt 011: to **PacketReceived** state on a *CrcOk* interrupt. If CRC is wrong (corrupted packet, with CRC on but CrcAutoClearOn is off), the PayloadReady interrupt will drive the sequencer to RxTimeout state. 100: to **SequencerOff** state on a *Rssi* interrupt 101: to **SequencerOff** state on a *SyncAddress* interrupt 110: to **SequencerOff** state on a *PreambleDetect* interrupt Irrespective of this setting, transition to **LowPowerSelection** on a *T2* interrupt
FromRxTimeout	Controls the state-machine transition from the **Receive** state on a *RxTimeout* interrupt (and on *PayloadReady* if **FromReceive** = 011): 00: to **Receive** state via *ReceiveRestart* 01: to **Transmit** state 10: to **LowPowerSelection** 11: to **SequencerOff** state Note: RxTimeout interrupt is a *TimeoutRxRssi*, *TimeoutRxPreamble* or *TimeoutSignalSync* interrupt.
FromPacketReceived	Controls the state-machine transition from the **PacketReceived** state: 000: to **SequencerOff** state 001: to **Transmit** on a *FifoEmpty* interrupt 010: to **LowPowerSelection** 011: to **Receive** via *FS* mode, if frequency was changed 100: to **Receive** state (no frequency change)

Table 20 Sequencer Transition Options

11.5.3. TIMERS

Two timers (Timer1 and Timer2) are also available in order to define periodic sequences. These timers are used to generate interrupts, which can trigger transitions of the Sequencer.

T1 interrupt is generated (Timer1Resolution * Timer1Coefficient) after T2 interrupt or SequencerStart. command.
T2 interrupt is generated (Timer2Resolution * Timer2Coefficient) after T1 interrupt.

The timers' mechanism is summarized on the following diagram.

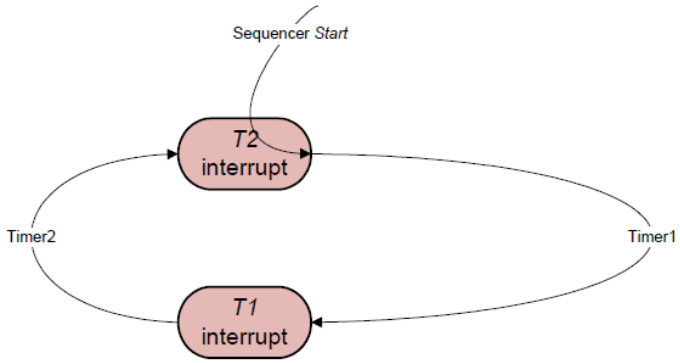


Figure 12 Timer1 and Timer2 Mechanism

***Note**: The timer sequence is completed independently of the actual Sequencer state. Thus, both timers need to be on to achieve periodic cycling.*

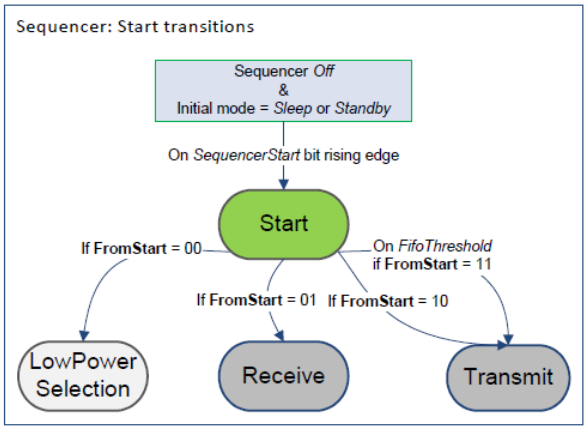
Variable	Description
Timer1Resolution	Resolution of Timer1 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms
Timer2Resolution	Resolution of Timer2 00: disabled 01: 64 us 10: 4.1 ms 11: 262 ms
Timer1Coefficient	Multiplying coefficient for Timer1
Timer2Coefficient	Multiplying coefficient for Timer2

Table 21 Sequencer Timer Settings

11.5.4. SEQUENCER STATE MACHINE

The following graphs summarize every possible transition between each Sequencer state. The Sequencer states are highlighted in grey. The transitions are represented by arrows. The condition activating them is described over the transition arrow. For better readability, the start transitions are separated from the rest of the graph.

Transitory states are highlighted in light grey, and exit states are represented in red. It is also possible to force the Sequencer off by setting the Stop bit in RegSeqConfig1 to 1 at any time.



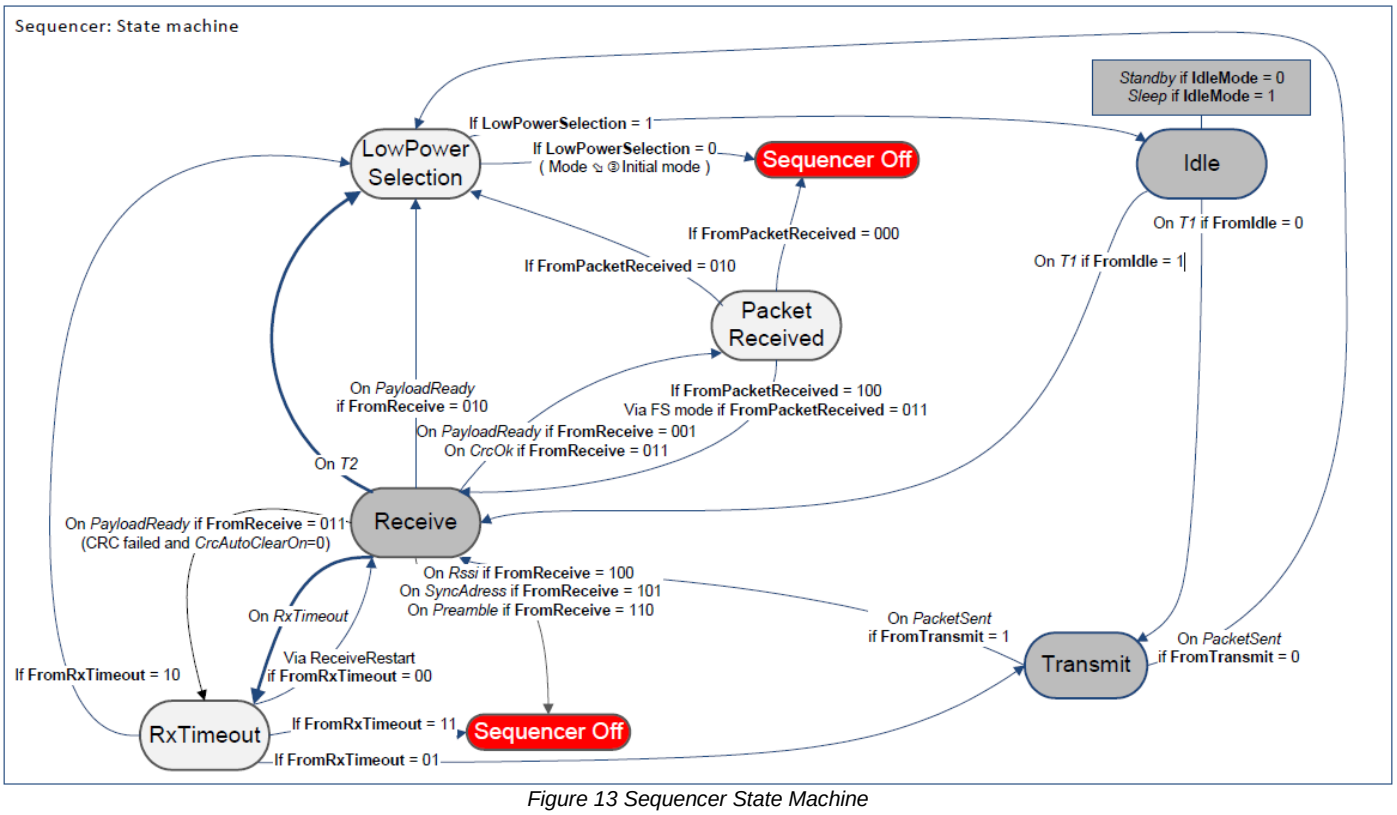


Figure 13 Sequencer State Machine

12. PACKET FORMAT

12.1. FIXED LENGTH PACKET FORMAT

Fixed length packet format is selected when bit PacketFormat is set to 0 and PayloadLength is set to any value greater than 0.

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF overhead (no length byte field is required). All nodes, whether Tx only, Rx only, or Tx/Rx should be programmed with the same packet length value.

The length of the payload is limited to 2047 bytes.

The length programmed in PayloadLength relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

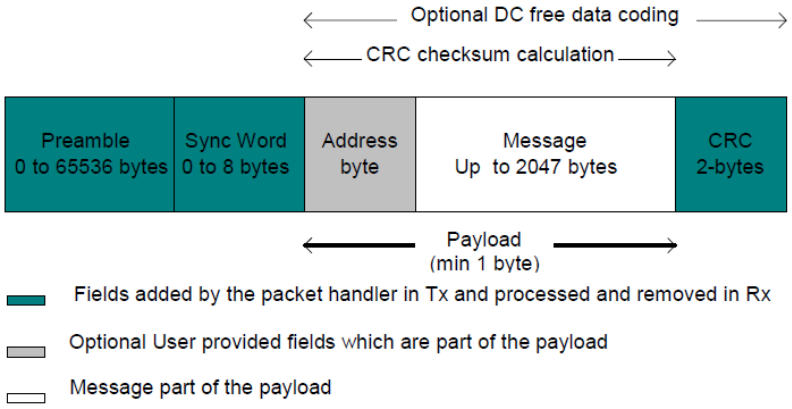


Figure 14 Fixed Length Packet Format

12.2. VARIABLE LENGTH PACKET FORMAT

Variable length packet format is selected when bit PacketFormat is set to 1.

This mode is useful in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.

In this mode the length of the payload, indicated by the length byte, is given by the first byte of the FIFO and is limited to 255 bytes. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Length byte
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

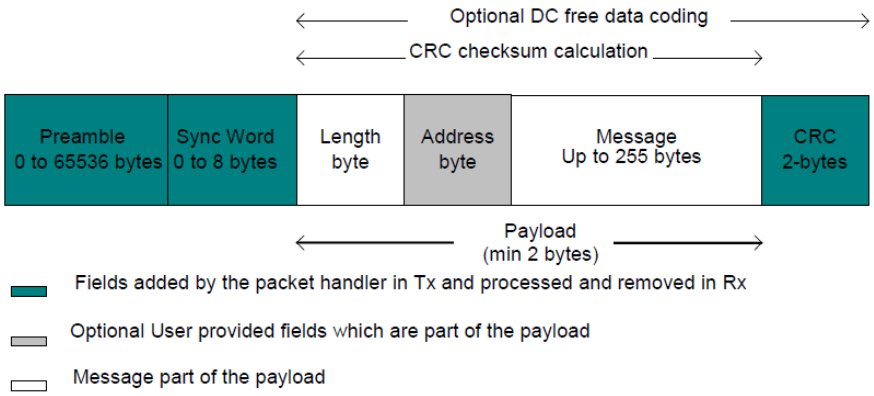


Figure 15 Variable Length Packet Format

12.3. UNLIMITED LENGTH PACKET FORMAT

Unlimited length packet format is selected when bit PacketFormat is set to 0 and PayloadLength is set to 0.

The user can then transmit and receive packet of arbitrary length and PayloadLength register is not used in Tx/Rx modes for counting the length of the bytes transmitted/received.

In Tx the data is transmitted depending on the TxStartCondition bit. On the Rx side the data processing features like Address filtering, Manchester encoding and data whitening are not available if the sync pattern length is set to zero (SyncOn = 0). The filling of the FIFO in this case can be controlled by the bit FifoFillCondition. The CRC detection in Rx is also not supported in this mode of the packet handler, however CRC generation in Tx is operational. The interrupts like CrcOk & PayloadReady are not available either.

An unlimited length packet shown below is made up of the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Optional Address byte (Node ID).
- Message data
- Optional 2-bytes CRC checksum (Tx only)

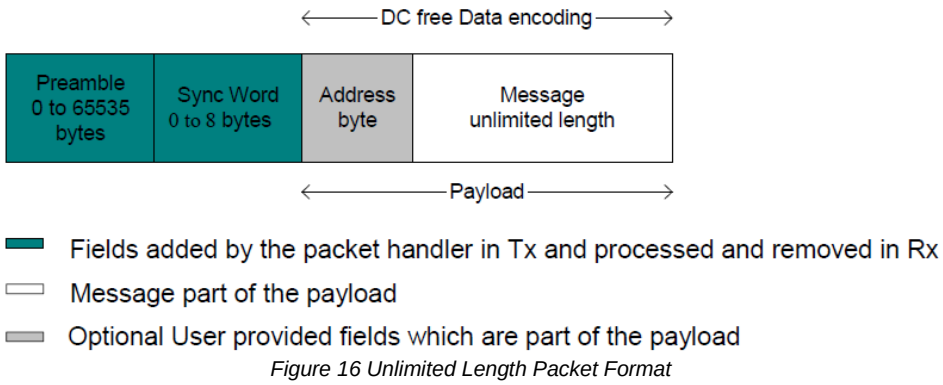
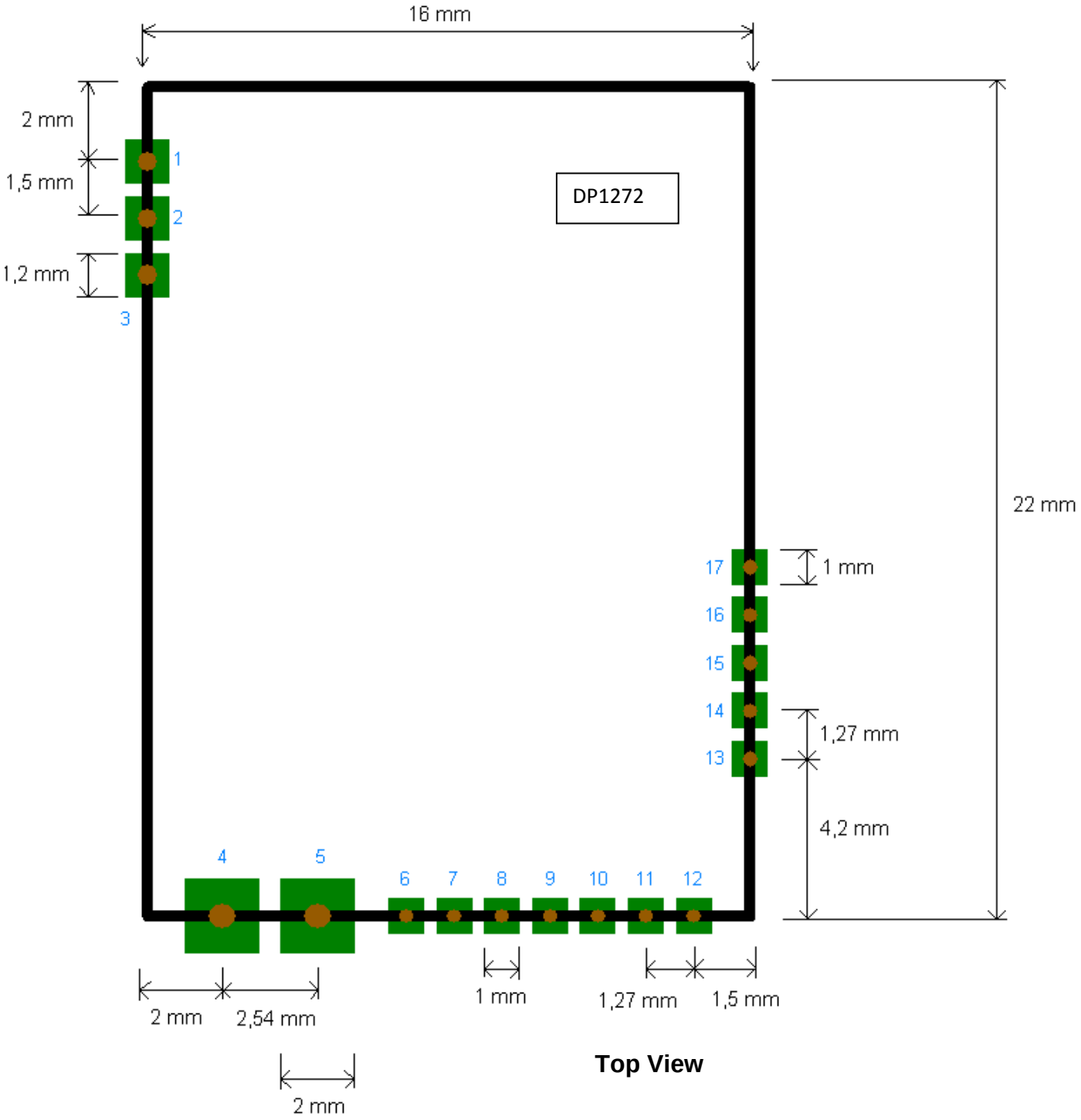


Figure 16 Unlimited Length Packet Format

13. MECHANICAL DIMENSIONS

The following drawing shows the physical footprint and dimensions of the DP1272 drop-in module.



Top View

Version	Create Date:	Creater	Changes
01	25.11.13	M.H.	Release Datasheet
02	02.06.14	M.H.	Value Corrections

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