

## DP1231 – C315/C433/C868/C915

### 315, 433, 868 and 915 MHz Drop-In RF Transceiver Modules Combine Small Form Factor with High Performance

#### GENERAL DESCRIPTION

The DP1231 is a low cost transceiver module operating in the frequency ranges from 290-340 MHz, 424-510, 862-1020 MHz. The DP1231 is optimized for High Link Budget and for very small form factor. It incorporates a baseband modem with data rates up to 300 kb/s. Data handling features include a 66 byte FIFO, packet handling, automatic CRC generation and data whitening. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC part 15) regulatory standards.

#### APPLICATIONS

- Wireless alarm and security systems
- Wireless sensor networks
- Automated Meter Reading
- Home and building automation
- Industrial monitoring and control

#### KEY PRODUCT FEATURES

- High Sensitivity: down to -120 dBm at 1.2 kbps
- High Selectivity: 16-tap FIR Channel Filter
- Bullet-proof front end: IIP3 = -18 dBm, IIP2 = 35dBm, 80 dB Blocking Immunity
- FSK, GFSK, MSK, GMSK and OOK modulations
- Constant RF performance from 1.8 to 3.6 Volt
- FSK Bit rates up to 300 kb/s
- Programmable RF output power: up to +13 dBm in 1 dB steps starting from -18 dBm
- Low current: Rx = 16 mA, 100nA register retention
- Fully integrated synthesizer with a resolution of 61 Hz
- Built-in Bit Synchronizer performing Clock Recovery
- Incoming Sync Word Recognition
- 115 dB+ Dynamic Range RSSI
- Automatic RF Sense with ultra-fast AFC
- Packet engine with CRC, AES-128 encryption and 66-byte FIFO
- Built-in temperature sensor and Low Battery indicator

#### DEVICE OPTIONS

Part	Frequency band	Pin Package
DP1231C315	290 - 340 MHz	Board
DP1231C433	424 - 510 MHz	Board
DP1231C868	862 - 902 MHz	Board
DP1231C915	902 - 1020 MHz	Board

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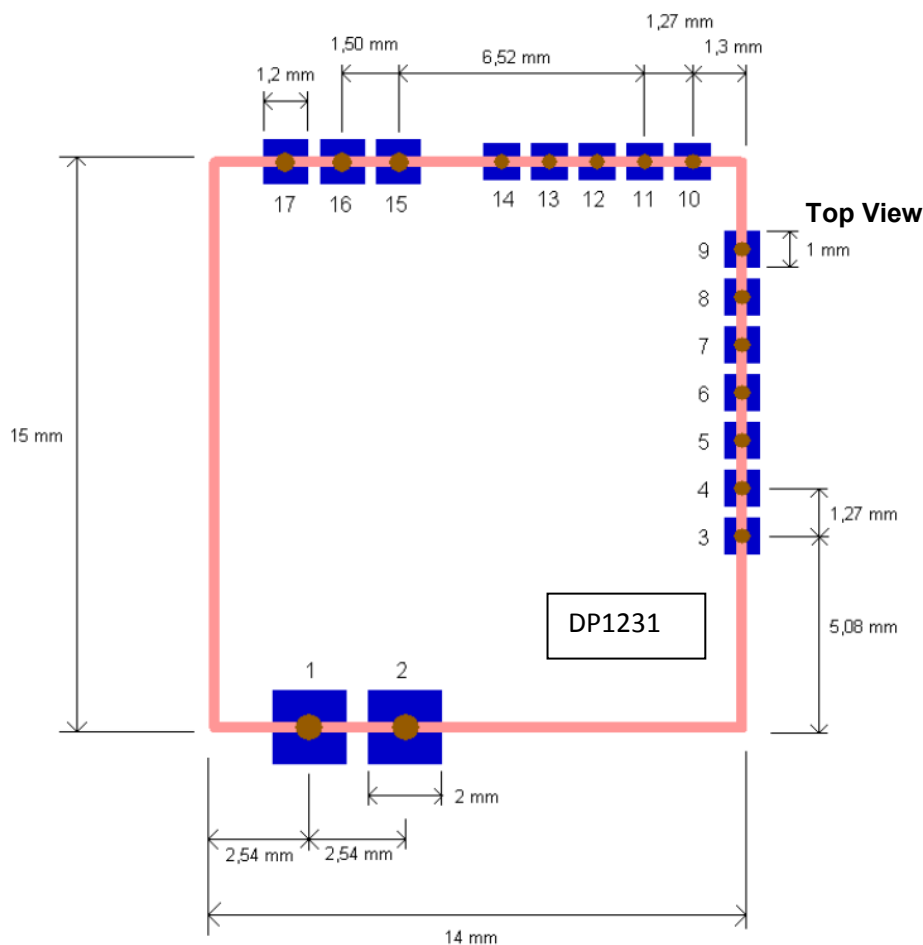
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### 1. PIN DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	GND		Ground
2	VCC		Supply Voltage
3	RESET	IN/OUT	Reset trigger input
4	DIO0	IN/OUT	Digital I/O, software configured
5	DIO1/DCLK	IN/OUT	Digital I/O, software configured
6	DIO2/DATA	IN/OUT	Digital I/O, software configured
7	DIO3	IN/OUT	Digital I/O, software configured
8	DIO4	IN/OUT	Digital I/O, software configured
9	DIO5	IN/OUT	Digital I/O, software configured
10	SCK	IN	SPI Clock input
11	MISO	OUT	SPI Data output
12	MOSI	IN	SPI Data input
13	NSS	IN	SPI Chip select input
14	RXTX	OUT	Rx/Tx switch control: high in Tx – Mode
15	GND		Ground
16	RF_IN_OUT	IN/OUT	RF Input / Output terminal
17	GND		Ground

**2. ELECTRICAL CHARACTERISTICS**

**2.1. ABSOLUTE MAXIMUM OPERATING RANGES**

Description	Min	Max	Unit
Supply voltage	1.8	3.6	V
Operating temperature	-10	+60	°C
Storage temperature	-55	125	°C
Soldering temperature (max 15 sec)		260	°C



CAUTION: ESD sensitive device.  
Precaution should be taken when handling the device in order to prevent permanent damage



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## 2.2. SPECIFICATIONS

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VDD=3.3 V, temperature = 25 °C, FXOSC = 32 MHz, FRF = 915 MHz, Pout = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FR	Synthesizer Frequency Range	DP1231-C315	290	-	340	MHz
		DP1231-C433	424	-	510	MHz
		DP1231-C868	862	-	902	MHz
		DP1231-C915	902	-	1020	MHz

IDDSL	Supply current in Sleep mode		-	0.1	1	µA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	µA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.25	1.5	mA
IDDFS	Supply current in Synthesizer mode		-	9	-	mA
IDDR	RX mode supply current		-	16	-	mA
IDDT	TX mode supply current	RFOP = +13 dBm	-	45	-	mA
		RFOP = +10 dBm	-	33	-	mA
		RFOP = 0 dBm	-	20	-	mA
		RFOP = -1 dBm	-	16	-	mA

RFS_F	RF Sensitivity (FSK)	FDA=5kHz, BR = 1.2kb/s*	-	-120	-	dBm
		FDA=5kHz, BR = 4.8kb/s	-	-114	-	dBm
		FDA=40kHz, BR=38.4kb/s	-	-105	-	dBm
RFS_O	RF Sensitivity (OOK)	BR = 4.8 kb/s	-	-112	-109	dBm

FDA	Frequency Deviation	Programmable FDA + BRF/2=<500kHz	0.6	-	300	kHz
BR_F	Bit rate (FSK)	Programmable	1.2	-	300	kb/s
BR_O	Bit rate (OOK)	Programmable	1.2	-	32.768	kb/s

RFOP	RF output power, programmable in 1dB steps	Programmable.	-18		+13	dBm
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TS_TR	Transmitter wake-up time, to the first rising edge of DCLK	Frequency Synthesizer on, PaRamp=10µs, BR=4.8kb/s	-	120	-	µs
TS_RE	Receiver wake up time, from PLL locked state to RXReady	RxBw=10kHz, BR=4.8kb/s	-	1.7	-	Ms
		RxBw=200kHz, BR=100kb/s	-	96	-	µs
TS_OSC	Quartz oscillator wake up time		-	250	500	µs

XTAL	Quartz oscillator frequency			32		MHz
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\*Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver

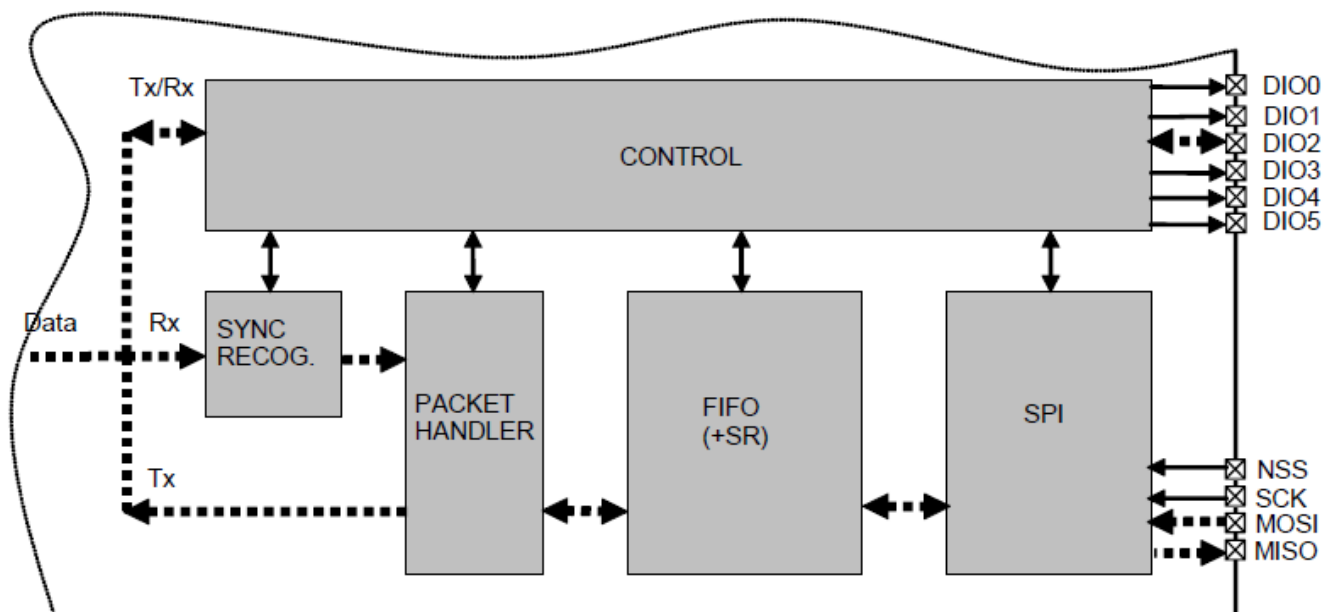
### 3. FUNCTIONAL DESCRIPTION

The DP1231 is a cost effective high performance radio transceiver module designed for the wireless transmission of digital information.

The module is based on the RF transceiver SX1231 from Semtech. For more information on the SX1231, please refer to the datasheet, available from the Semtech website:

<http://www.semtech.com> .

Figure below illustrates the SX1231 data processing circuit. Its role is to interface the data to/from the modulator/demodulator and the  $\mu$ C access points (SPI and DIO pins). It also controls all the configuration registers.



..... Potential datapaths (data operation mode dependant)

Figure 1

### 4. DATA OPERATION MODES

The DP1231 has two different data operation modes selectable by the user:

Continuous mode: each bit transmitted or received is accessed in real time at the DIO2/DATA pin. This mode may be used if adequate external signal processing is available.

Packet mode (recommended): user only provides/retrieves payload bytes to/from the FIFO. The packet is automatically

built with preamble, Sync word, and optional AES, CRC, and DC-free encoding schemes. The reverse operation is performed in reception. The  $\mu$ C processing overhead is hence significantly reduced compared to Continuous mode. Depending on the optional features activated (CRC, AES, etc) the maximum payload length is limited to FIFO size, 255 bytes or unlimited.

For more information about the data operation modes, please refer to the SX1231 datasheet chapter: *Description*. You can find this at <http://www.semtech.com> .

## 5. Digital IO Pins Mapping

Six general purpose IO pins are available on the SX1231, and their configuration in Continuous or Packet mode is controlled through *RegDioMapping1* and *RegDioMapping2*.

### 5.1 DIO Pins Mapping in Continuous Mode

Mode	Diox Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
Sleep	00	-	-	-	-	-	-
	01	-	-	-	-	-	-
	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	-	-	-	-	ModeReady
Stdby	00	ClkOut	-	-	-	-	-
	01	-	-	-	-	-	-
	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	-	-	-	-	ModeReady
FS	00	ClkOut	-	-	-	-	PIILock
	01	-	-	-	-	-	-
	10	LowBat	LowBat	AutoMode	-	LowBat	LowBat
	11	ModeReady	PIILock	-	-	PIILock	ModeReady
Rx	00	ClkOut	Timeout	Rssi	Data	Dclk	SyncAddress
	01	Rssi	RxReady	RxReady	Data	RxReady	Timeout
	10	LowBat	SyncAddress	AutoMode	Data	LowBat	Rssi
	11	ModeReady	PIILock	Timeout	Data	SyncAddress	ModeReady
Tx	00	ClkOut	TxReady	TxReady	Data	Dclk	PIILock
	01	ClkOut	TxReady	TxReady	Data	TxReady	TxReady
	10	LowBat	LowBat	AutoMode	Data	LowBat	LowBat
	11	ModeReady	PIILock	TxReady	Data	PIILock	ModeReady

Figure 2

### 5.2 DIO Pins Mapping in Packet Mode

Mode	Diox Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
Sleep	00	-	-	FifoFull	FifoNotEmpty	FifoLevel	-
	01	-	-	-	-	FifoFull	-
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	-	-	AutoMode	-	-
Stdby	00	ClkOut	-	FifoFull	FifoNotEmpty	FifoLevel	-
	01	-	-	-	-	FifoFull	-
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	-	-	AutoMode	-	-
FS	00	ClkOut	-	FifoFull	FifoNotEmpty	FifoLevel	-
	01	-	-	-	-	FifoFull	-
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PIILock	PIILock	AutoMode	PIILock	PIILock
Rx	00	ClkOut	Timeout	FifoFull	FifoNotEmpty	FifoLevel	CrcOk
	01	Data	Rssi	Rssi	Data	FifoFull	PayloadReady
	10	LowBat	RxReady	SyncAddress	LowBat	FifoNotEmpty	SyncAddress
	11	ModeReady	PIILock	PIILock	AutoMode	Timeout	Rssi
Tx	00	ClkOut	ModeReady	FifoFull	FifoNotEmpty	FifoLevel	PacketSent
	01	Data	TxReady	TxReady	Data	FifoFull	TxReady
	10	LowBat	LowBat	LowBat	LowBat	FifoNotEmpty	LowBat
	11	ModeReady	PIILock	PIILock	AutoMode	PIILock	PIILock

Figure 3

For more information about the data operation modes, please refer to the SX1231 datasheet chapter: *Description*. You can find this on <http://www.semtech.com>.

## 6. SPI Interface description

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL= 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Three access modes to the registers are provided:

- **SINGLE access:** an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the begin of the frame and goes high after the data byte.
- **BURST access:** the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.
- **FIFO access:** if the address byte corresponds to the address of the FIFO, then succeeding data byte will address the FIFO. The address is not automatically incremented but is memorized and does not need to be sent between each data byte. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

Figure below shows a typical SPI single access to a register.

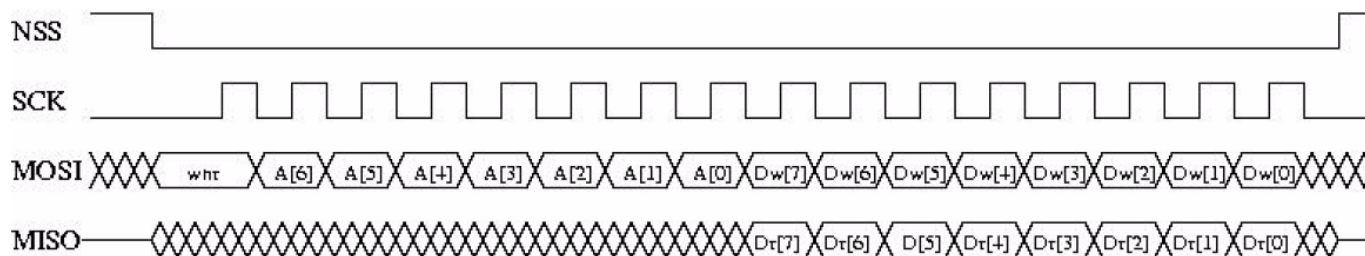


Figure 4

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer always starts by the NSS pin going low. MISO is high impedance when NSS is high.

For more information about the serial interface, please refer to the SX1231 datasheet chapter: *Control Block Description*. You can find this at <http://www.semtech.com>.

## 7. OPERATING MODES

The circuit can be set in 5 different basic modes which are described in Table 14.

By default, when switching from a mode to another one, the sub-blocks are woken up according to a pre-defined and optimized sequence. Alternatively, these operating modes can be selected directly by disabling the automatic sequencer (*SequencerOff* in *RegOpMode* = 1).

ListenOn in RegOpMode	Mode in RegOpMode	Selected Mode	Enabled blocks
0	000	Sleep Mode	None
0	001	Stand-by Mode	Top regulator and crystal oscillator
0	010	FS Mode	Frequency synthesizer
0	011	Transmit Mode	Frequency synthesizer and transmitter
0	100	Receive Mode	Frequency synthesizer and receiver
1	x	Listen Mode	See Listen Mode (7.1)

### 7.1 Listen Mode

The circuit can be set to Listen mode, by setting *ListenOn* in *RegOpMode* to 1. In this mode, SX1231 spends most of the time in Idle mode, during which only the RC oscillator runs. Periodically the receiver is woken up and listens for an RF signal. If a wanted signal is detected, the receiver is kept on and the data is demodulated.

Otherwise, if a wanted signal hasn't been detected after a pre-defined period of time, the receiver is disabled until the next time period.

This periodical Rx wake-up requirement is very common in low power applications. On SX1231 it is handled locally by the Listen mode block without using uC resources or energy.

The simplified timing diagram of this procedure is illustrated in Figure 1.

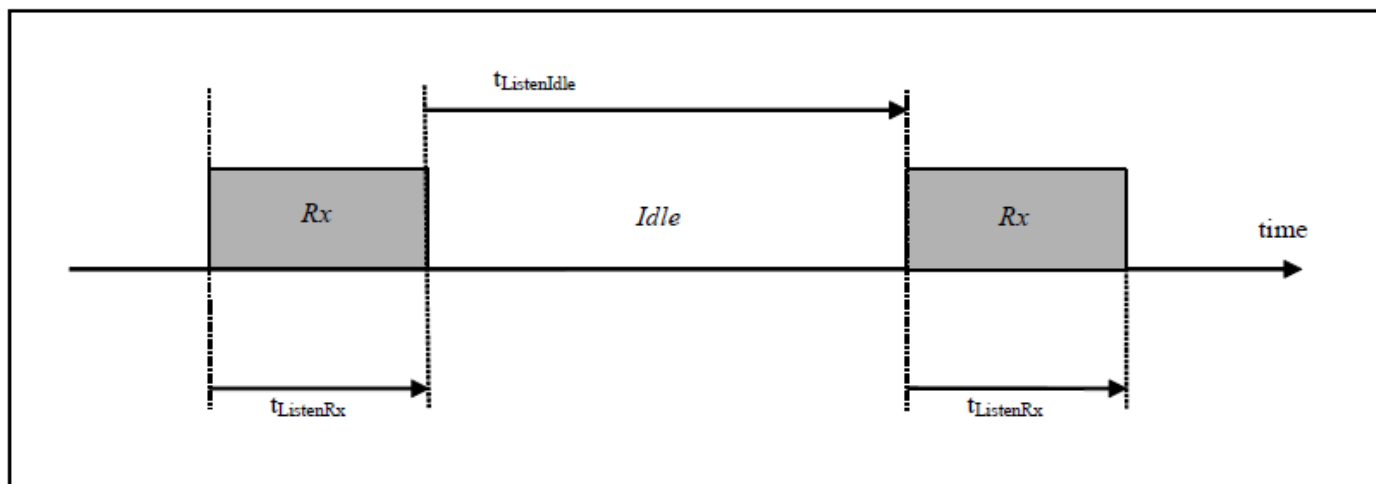


Figure 5

For more information about the modes of operation, please refer to the SX1231 Datasheet on the Semtech website <http://www.semtech.com>.

## 8. Packet Format

### 8.1. Fixed Length Packet Format

Fixed length packet format is selected when bit PacketFormat is set to 0 and PayloadLength is set to any value greater than 0.

In applications where the packet length is fixed in advance, this mode of operation may be of interest to minimize RF Overhead (no length byte field is required). All nodes, whether Tx only, Rx only, or Tx/Rx should be programmed with the same packet length value.

The length of the payload is limited to 255 bytes if AES is not enabled else the message is limited to 64 bytes ( i.e. max 65 bytes payload if Address byte is enabled ).

The length programmed in PayloadLength relates only to the payload which includes the message and the optional address byte. In this mode, the payload must contain at least one byte, i.e. address or message byte.

An illustration of a fixed length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

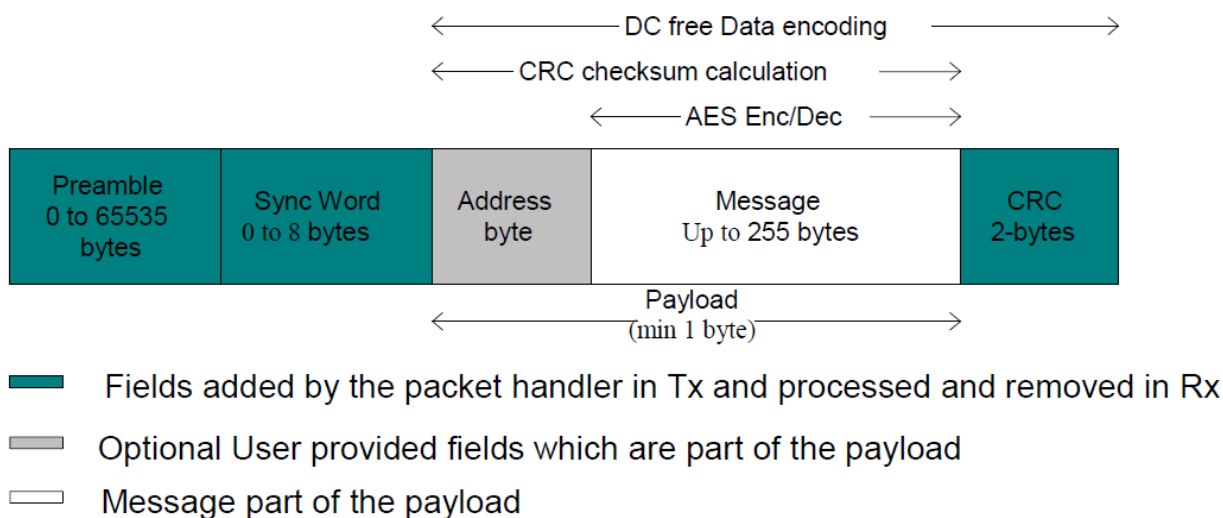


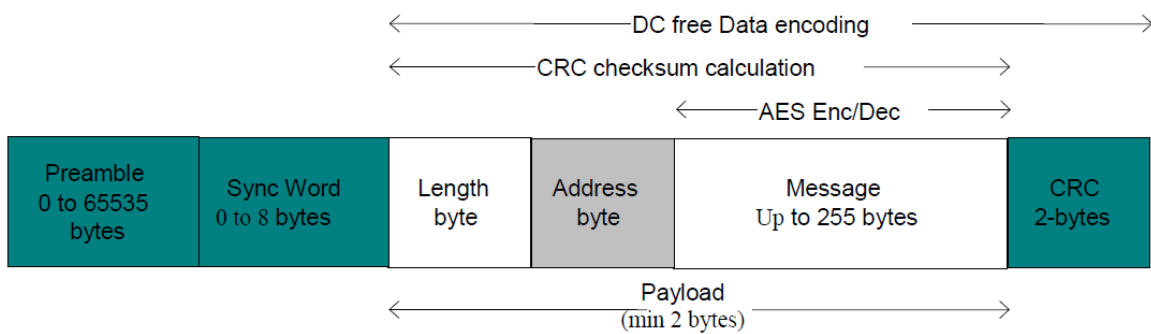
Figure 6, Fixed Length Packet Format

### 8.2. Variable Length Packet Format

Variable length packet format is selected when bit PacketFormat is set to 1. This mode is useful in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly. In this mode the length of the payload, indicated by the length byte, is given by the first byte of the FIFO and is limited to 255 bytes if AES is not enabled else the message is limited to 64 bytes i.e. max 66 bytes payload if Address byte is enabled. Note that the length byte itself is not included in its calculation. In this mode, the payload must contain at least 2 bytes, i.e. length + address or message byte.

An illustration of a variable length packet is shown below. It contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Length byte
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum



- Fields added by the packet handler in Tx and processed and removed in Rx
- Optional User provided fields which are part of the payload
- Message part of the payload

Figure 7, Variable Length Packet Format

### 8.3. Unlimited Length Packet Format

Unlimited length packet format is selected when bit PacketFormat is set to 0 and PayloadLength is set to 0. The user can then transmit and receive packet of arbitrary length and PayloadLength register is not used in Tx/Rx modes for counting the length of the bytes transmitted/received. This mode is a replacement for the legacy buffered mode in DPS1211 Modules. In Tx the data is transmitted depending on the TxStartCondition bit. On the Rx side the data processing features like Address filtering, Manchester encoding and data whitening are not available if the sync pattern length is set to zero (SyncOn = 0). The filling of the FIFO in this case can be controlled by the bit FifoFillCondition. The CRC detection in Rx is also not supported in this mode of the packet handler, however CRC generation in Tx is operational. The interrupts like CrcOk & PayloadReady are not available either.

An unlimited length packet shown in is made up of the following fields:

- Preamble (1010...).
- Sync word (Network ID).
- Optional Address byte (Node ID).
- Message data
- Optional 2-bytes CRC checksum (Tx only)

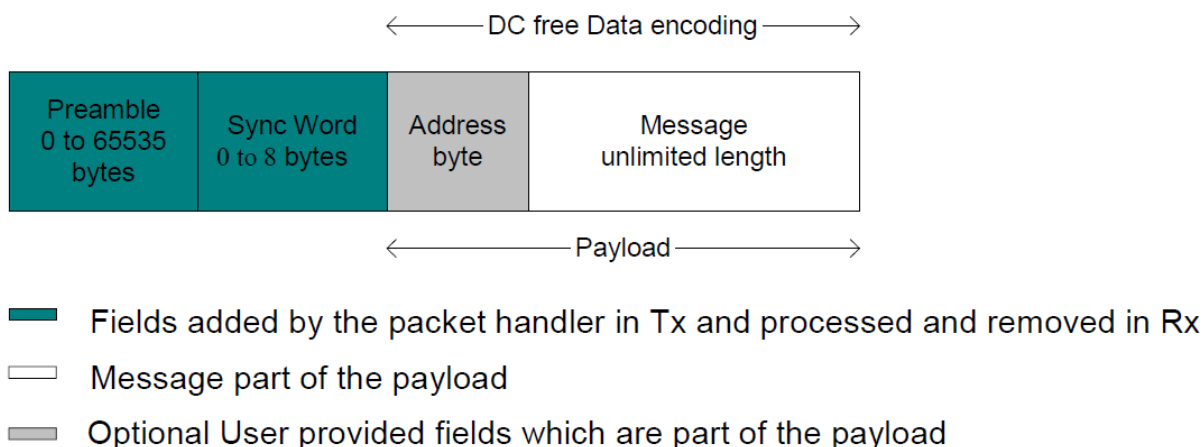


Figure 8, Unlimited Length Packet Format

## 9. AES

AES is the symmetric-key block cipher that provides the cryptographic capabilities to the transceiver. The system proposed can work with 128-bit long fixed keys. The fixed key is stored in a 16-byte write only user configuration register, which retains its value in Sleep mode. As shown in Figure 31 and Figure 32 above the message part of the Packet can be encrypted and decrypted with the cipher 128- cipher key stored in the configuration registers.

### 9.1. Tx Processing

1. User enters the data to be transmitted in FIFO in Stdby/Sleep mode and gives the transmit command.
2. On Tx command the Packet handler state machine takes over the control and If encryption is enabled then the message inside the FIFO is read in blocks of 16 bytes (padded with 0s if needed), encrypted and stored back to FIFO. All this processing is done in Tx mode before enabling the packet handling state machine. Only the Message part of the packet is encrypted and preamble, sync word, length byte, address byte and CRC are not encrypted.
3. Once the encryption is done the Packet handling state machine is enabled to transmit the data.

### 9.2. Rx Processing

1. The data received is stored in the FIFO, The address, CRC interrupts are generated as usual because these parameters were not encrypted.
2. Once the complete packet has been received. The data is read from the FIFO, decrypted and written back to FIFO. The PayloadReady interrupt is issued once the decrypted data is ready in the FIFO for reading via the SPI interface. The AES encryption/decryption cannot be used on the fly i.e. while transmitting and receiving data. Thus when AES encryption/decryption is enabled, the FIFO acts as a simple buffer. This buffer is filled before initiating any transmission. The data in the buffer is then encrypted before the transmission can begin. On the receive side the decryption is initiated only once the complete packet has been received in the buffer. The encryption/decryption process takes approximately 7.0 us per 16-byte block. Thus for a maximum of 4 blocks (i.e. 64 bytes) it can take up to 28 us for completing the cryptographic operations. The receive side sees the AES decryption time as a sequential delay before the PayloadReady interrupt is available. The Tx side sees the AES encryption time as a sequential delay in the startup of the Tx chain, thus the startup time of the Tx will increase according to the length of data.

In Fixed length mode the Message part of the payload that can be encrypted/decrypted can be 64 bytes long. If the address filtering is enabled, the length of the payload should be at max 65 bytes in this case.

In Variable length mode the Max message size that can be encrypted/decrypted is also 64 bytes when address filtering is disabled, else it is 48 bytes. Thus, including length byte, the length of the payload is max 65 or 50 bytes (the latter when address filtering is enabled). If the address filtering is expected then AddressFiltering must be enabled on the transmitter side as well to prevent address byte to be encrypted.

CRC check being performed on encrypted data, CrcOk interrupt will occur "decryption time" before PayloadReady interrupt.

10. Bit Rate Examples

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual BR (b/s)
Classical modem baud rates (multiples of 1.2 kbps)	0x68	0x2B	1.2 kbps	1.2 kbps	1200.015
	0x34	0x15	2.4 kbps	2.4 kbps	2400.060
	0x1A	0x0B	4.8 kbps	4.8 kbps	4799.760
	0x0D	0x05	9.6 kbps	9.6 kbps	9600.960
	0x06	0x83	19.2 kbps	19.2 kbps	19196.16
	0x03	0x41	38.4 kbps		38415.36
	0x01	0xA1	76.8 kbps		76738.60
	0x00	0xD0	153.6 kbps		153846.1
Classical modem baud rates (multiples of 0.9 kbps)	0x02	0x2C	57.6 kbps		57553.95
	0x01	0x16	115.2 kbps		115107.9
Round bit rates (multiples of 12.5, 25 and 50 kbps)	0x0A	0x00	12.5 kbps	12.5 kbps	12500.00
	0x05	0x00	25 kbps	25 kbps	25000.00
	0x02	0x80	50 kbps		50000.00
	0x01	0x40	100 kbps		100000.0
	0x00	0xD5	150 kbps		150234.7
	0x00	0xA0	200 kbps		200000.0
	0x00	0x80	250 kbps		250000.0
	0x00	0x6B	300 kbps		299065.4
Watch Xtal frequency	0x03	0xD1	32.768 kbps	32.768 kbps	32753.32

Figure 9

### 11. MECHANICAL DIMENSIONS

The following drawing shows the physical footprint and dimensions of the DP1231 drop-in module.

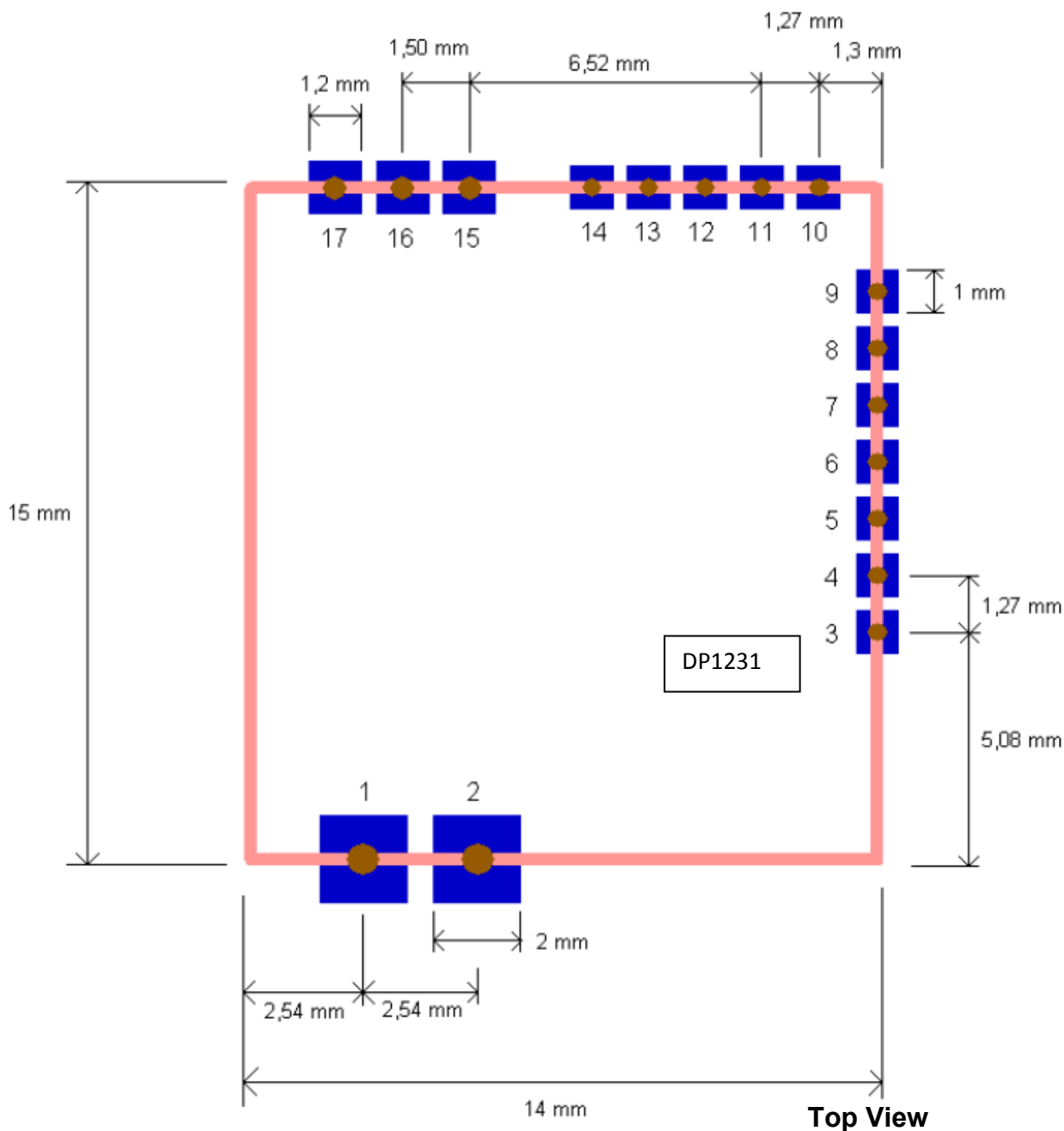


Figure 10

**WIRELESS PRODUCTS**

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Version	Create Date:	Creator	Changes
01	24.10.2012	Goldmann	Release first Datasheet

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