DP1205 – C433/C868/C915

433, 868 and 915 MHz Drop-In RF Transceiver Modules

Combine Small Form Factor with High Performance

GENERAL DESCRIPTION

The DP1205s are complete Radio Transceiver Modules operating in the 433, 868 and 915 MHz license free ISM (Industrial Scientific and Medical) frequency bands. Based on the XE1205 transceiver from Semtech, the DP1205 offers the unique advantage of narrow-band and wide-band communication. Offering high output power and exceptional receiver sensitivity, the radio module is suitable for applications seeking to satisfy the European (ETSI EN300-220-1) or the North American (FCC part 15) regulatory standards.

The DP1205 is suitable for operation in the European social alarm bands (25 kHz channel spacing). Its built-in 16-byte FIFO and full SPI simplify interfacing to the host controller.

APPLICATIONS

- Narrow-band and wide-band security systems
- Voice and data over an RF link
- Process and building control
- Access control
- Home automation
- Home appliance interconnections

KEY PRODUCT FEATURES

- No RF knowledge required to use
- Direct Digital interface
- Fully assembled and tested
- Surface mount
- 30.5 mm x 18.5 mm
- Supply voltage 2.4 V – 3.6 V
- Frequency synthesizer steps 500 Hz
- Output power is programmable up to 15 dBm
- High Rx sensitivity: down to -121 dBm at 1.2 kbit/s, -116 dBm at 4.8 kbit/s.
- Data rate up to 304.7 kbit/s
- Current consumption Tx=62 mA@15 dBm
- Current consumption Rx=14 mA
- 16-byte FIFO
- Digital RSSI (Received Signal Strength Indicator)
- Digital FEI (Frequency Error Indicator)

DEVICE OPTIONS

Part	Frequency band	Pin Package
DP1205C433LF	433 - 435MHz	Board
DP1205C868LF	863 - 870MHz	Board
DP1205C915LF	902 - 928MHz	Board

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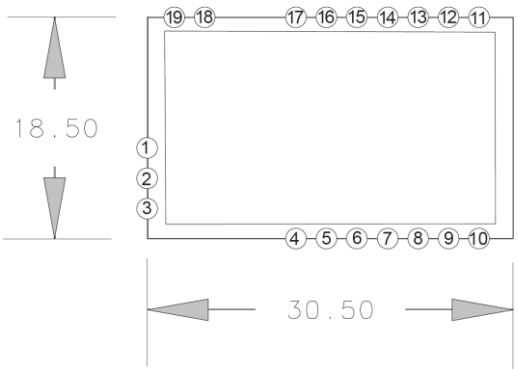
1. NON-CONFORMANCE

Please note that the leaded version of this product exhibits a non-conformance. The non-conformance affects the CLKOUT signal of the DP1205 which is not enabled at power-up of the module. It is also recommended to program all registers after power-up of the module. The Lead-Free version (suffix "LF") of this product does not exhibit these non-conformances.

Please note that all products whose date-codes are before 0706 (wwyy) exhibit a non-conformance to specification. The non-conformance affects the FIFO buffer of the XE1205 transceiver contained in this module as described in section 5 - Data operation modes. For these date-codes, please use the FIFO in this product only in conjunction with the Technical Note TN1205.01 (available from the SEMTECH web site). All other date-codes are in conformance with the specification.

2. PIN DESCRIPTION



PIN	NAME	I/O	DESCRIPTION
1	GND		Ground
2	RF_IN_OUT	IN/OUT	RF Input / Output terminal
3	GND		Ground
4	VDDA		Supply Voltage
5	GND		Ground
6	VDD		Supply Voltage
7	NSS_CONFIG	IN	SPI SELECT CONFIG
8	NSS_DATA	IN	SPI SELECT DATA / DATAIN
9	IRQ0	OUT	Interrupt (PATTERN//FIFOEMPTY)
10	GND		Ground
11	GND		Ground
12	IRQ1	OUT	Interrupt(DCLK/FIFOFULL)
13	DATA	IN/OUT	Data
14	CLKOUT	OUT	Output clock at reference frequency divided by 2, 4, 8, 16, 32
15	MISO	OUT	SPI Master Input Slave Output
16	MOSI	IN	SPI Master Output Slave Input
17	SCK	IN	SPI CLOCK
18	SW(0)	IN/OUT	Transmit/Receive/Stand-by/Sleep Mode Select
19	SW(1)	IN/OUT	Transmit/Receive/Stand-by/Sleep Mode Select

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3. ELECTRICAL CHARACTERISTICS

3.1. ABSOLUTE MAXIMUM OPERATING RANGES

Description	Min	Max	Unit
Supply voltage	2.4	3.6	V
Operating temperature	-40	+85	°C
Storage temperature	-55	125	°C
Soldering temperature (max 15 sec)		260	°C

CAUTION: ESD sensitive device.
Precaution should be taken when handling the device in order to prevent permanent damage

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3.2. SPECIFICATIONS

The table below gives the specifications of the DP1205 modules under the following conditions:
Supply Voltage = 3.3V, temperature = 25 °C, 2-level FSK without pre-filtering, fc = 915 MHz, Δf = 5 kHz,
Bit rate = 4.8 kbit/s, BW_{SSB} = 10 kHz, BER = 0.1% (at the output of the bit synchronizer), matched impedances, environment as defined in section 8 (Semtech XE1205 Datasheet), unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FR	Synthesizer Frequency Range	DP1205-C433	433	-	435	MHz
		DP1205-C868	863	-	870	MHz
		DP1205-C915	902	-	928	MHz
IDDSL	Sleep mode supply current		-	0.2	1	uA
IDDST	Standby mode supply current	39 MHz running	-	0.85	1.1	mA
IDDR	RX mode supply current			14	16.5	mA
IDDT	TX mode supply current	PRF = 5 dBm		33	40	mA
		PRF = 15dBm		62	75	mA
RFS	RF Sensitivity	A-Mode		-116	-113	dBm
RFS_12	RF Sensitivity at 1,2kbit/s	A-Mode / BER = 0.1 %		-121	-118	dBm
FDA	Frequency Deviation	Programmable	1	-	255	kHz
BR	Bit rate	Programmable	1.2	-	304.7[1)]	Kb/s
RFOP	RF output power	Programmable.				
		RFOP1	-3	0	-	dBm
		RFOP2	+2	+5	-	dBm
		RFOP3	+7	+10	-	dBm
		RFOP4	+12	+15	-	dBm
TS_STR	Transmitter wake-up time	From oscillator enabled	-	250	350	us
TS_SRE	Receiver wake up time	From oscillator enabled	-	700	850	us
TS_OS	Quartz oscillator wake up time	Fundamental	-	1	2	ms
XTAL	Quartz oscillator frequency			39		MHz
VIH	Digital input level high	% VDD	75	-	-	%
VIL	Digital input level low	% VDD	-	-	25	%

[1)] 304,7 kbit/s achievable with additionall register settings as described in section 6. The 304.7 kbit/s max bit rate is guaranteed by validation. The max bit rate guaranteed by production test is 152,3 kbit/s

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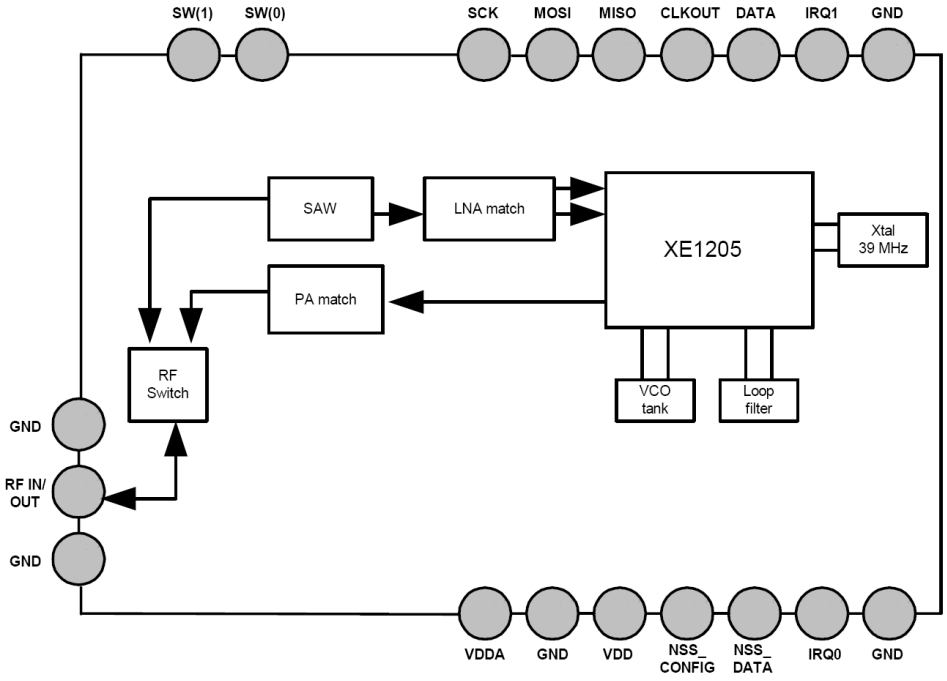
4. FUNCTIONAL DESCRIPTION

The TrueRF™ DP1205 is a cost effective high performance radio transceiver module designed for the wireless transmission of digital information over distances up to 8 km .

The module is based on the RF transceiver circuit from Semtech, the TrueRF XE1205. For more information on the XE1205, please refer to the datasheet, available from the Semtech website:
http://www.semtech.com .

The Module is also available with all high frequency circuits and the 39MHz reference crystal enclosed inside a shielding case. The Module also incorporates an antenna switch and a SAW Filter placed on the Rx path.



5. DATA OPERATION MODES

The XE1205 is user-programmable between two modes of operation:

Continuous mode: each bit transmitted or received is accessed directly at the DATA input/output pin.

Buffered mode: a 16-byte FIFO is used to store each data byte transmitted or received. This data is written to/read from the FIFO via the SPI bus. It reduces processor overhead and reduces connections (the DATA input/output pin is not used in this operation mode)

In receiver mode, two lines are dedicated to interrupt information. The interrupt pins are IRQ_0 and IRQ_1.
IRQ_0 has 3 selectable sources. IRQ_1 has 2 selectable sources. The two following tables summarize the interrupt management.

IRQParam_RX_irq_0	MCParam_Buffered_mode	IRQ_0	IRQ_0 Interrupt source
00	1	Output	No interrupt available
01	1	Output	Write_byte
10	1	Output	/fifoempty
11	1	Output	Pattern
00	0	Output	Pattern
01	0	Output	RSSI_irq
10	0	Output	Pattern
11	0	Output	Pattern

Table 1: IRQ_0 interrupt sources in receive mode.

IRQParam_RX_irq_1	MCParam_Buffered_mode	IRQ_1	IRQ_1 Interrupt source
00	1	Output	No interrupt available
01	1	Output	Fifofull
10	1	Output	RSSI_irq
11	1	Output	RSSI_irq
00	0	Output	DCLK
01	0	Output	DCLK
10	0	Output	DCLK
11	0	Output	DCLK

Table 2: IRQ_1 interrupt sources in receive mode.

For more information about the data operation modes, please refer to the XE1205 datasheet chapter: ***5 Description***
You can find this at http://www.semtech.com .

6. HIGHEST BIT RATES: EXAMPLE OF 304.7 KBIT/S OPERATION

XE1205 is able to sustain other bit rates between 152.34 kbit/s and 304.7 kbit/s using OSR_minus_1 register as described in section 5.2.3.2. It is recommended whenever possible to use a modulation index (β=2Δf/BR) ≥2 whenever possible. For the highest bit rates the receiver filter bandwidth will limit the maximal usuable β. Lower modulation indexes should be used then. In this chapter we provide the example of the highest bit rate.
In order to operate at 304.7 kbit/s the following settings should be used:
Please note that exact bitrate value is 304.6875 kbit/s.

6.1 Bitrate (BR) and frequency deviation (fdev)

At 304.7 kbit/s, a modulation index close to 1 is compulsory because of the limited bandwidth of the Rx filter. requency deviation will be set to 160 kHz to also take benefit from the Tx filter available (Cf Table 03).
Consequently, following settings should be programmed:

Name	Address	Bits	Value (d)	Note
0	0	Freq_dev(8:0)	1	7-0
320	160.36 kHz	Br(6:0)	2	6-0
0	152.34 kbit/s…	Chg_OSR	27	4
1	OSR (7:0)	28	7-0	15

Table 3: common registers settings for 304.7 kbit/s.

6.2 Rx filter

For a correct behavior we recommend to have an Rx filter bandwidth of minimum fdev + (BR/2).
Consequently, following settings should be programmed:

Name	Address	Bits	Value (d)	Note
BW(1:0)	8	6-5	3	200 kHz…
Max_BW	8	4	0	TParam_Low_BW
19	2	1	21	6-0
TParam_Code_BW(8:0)	22	7-6	87	…=>320 kHz

Table 4: Rx registers settings for 304.7 kbit/s

6.3 Tx filter

Tx filter is also available at 304.7 kbit/s operation and although not compulsory, its use is recommended to reduce spectrum bandwidth. Contrary to the other bitrates, an additional specific bit must be set.
Consequently, following settings should be programmed:

Name	**Address**	**Bits**	**Value (d)**	**Note**
Filter	7	4	1	304 kbit/s_filter
18	3	1		

Table 5: Tx registers settings for 304.7 kbit/s

6.4 HARDWARE SETTINGS

When operating at 304.7 kbit/s, the loop filter must be modified. Typical recommended component values are provided below :

Name	434 MHz	869 MHz	915 MHz	Tolerance
CL1	3.3 nF	10 nF	10 nF	± 5%
CL2	220 pF	150 pF	150 pF	± 5%
RL1	1.5 kÙ	1.5 kÙ	1.5 kÙ	± 5%

Table 6: PLL Loop Filter Bill of Material for 304.7 kbit/s

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6.5 OPERATION

Like for any other configuration, in order to avoid crystal misalignment issues and get the best performance it is recommended to perform an AFC with maximum Rx filter bandwidth before using the 304.7 kbit/s with the settings described above.

AFC operation may need to be performed at a lower datarate to cover worst case crystal, process and temperature variations.

Please note that all features including FIFO are available at bit rates up to 304.7 kbit/s.

6.6 TYPICAL PERFORMANCE

- Sensitivity@0.1%: -102 dBm in mode A and -90 dBm in mode B.
- ACR@1MHz offset, single tone: 25 dBc.

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6. SERIAL CONTROL INTERFACE

The XE1205 contains two SPI-compatible serial interfaces, one to send and read the chip configuration, the other to send and receive data in buffered mode. Both interfaces are configured in slave mode and share the same pins MISO (Master In Slave Out), MOSI (Master Out Slave In), SCK (Serial Clock). Two additional pins are required to select the SPI interface: NSS_config to change or read the transceiver configuration, and NSS_data to send or read data.

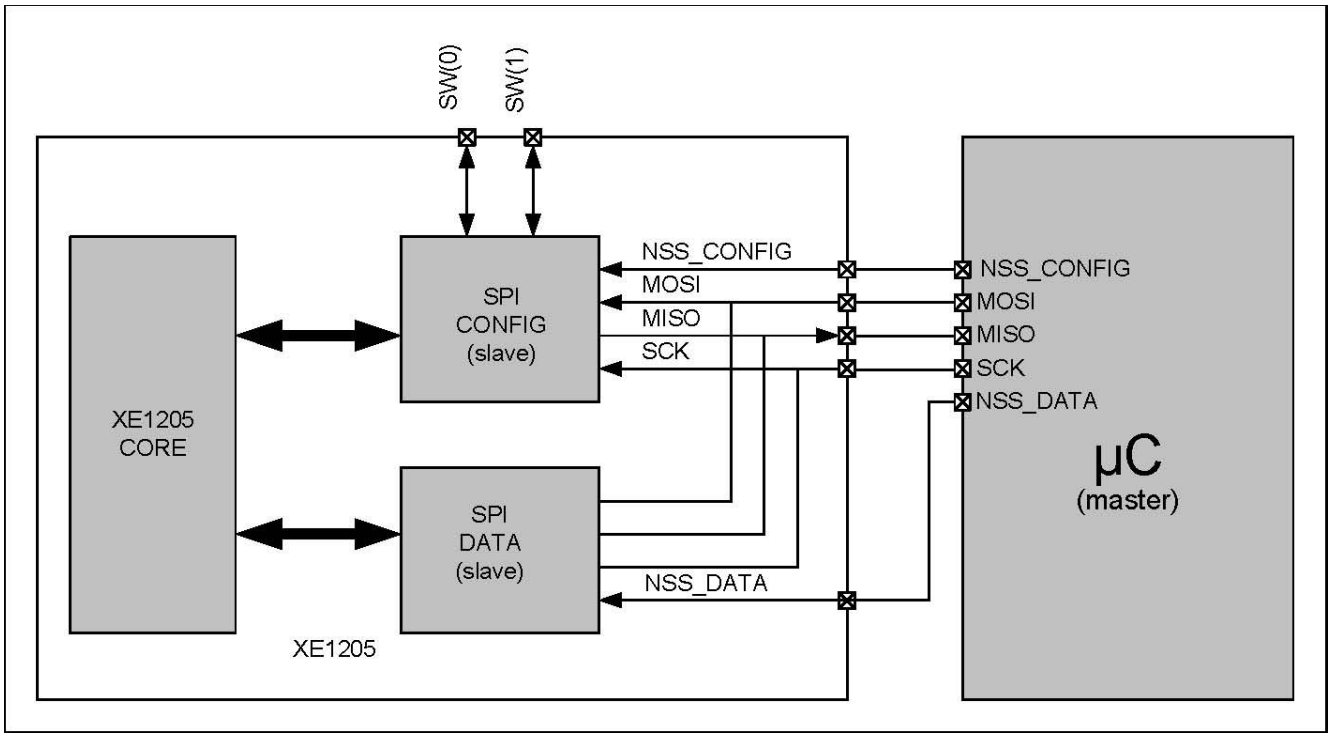


Figure 1 shows the connections between the transceiver and a microcontroller when buffered mode is used.

For more information about the serial interface, please refer to the XE1205 datasheet chapter: ***7 Serial Interface definition and principle of operation***.
You can find this at http://www.semtech.com .

7. OPERATING MODES

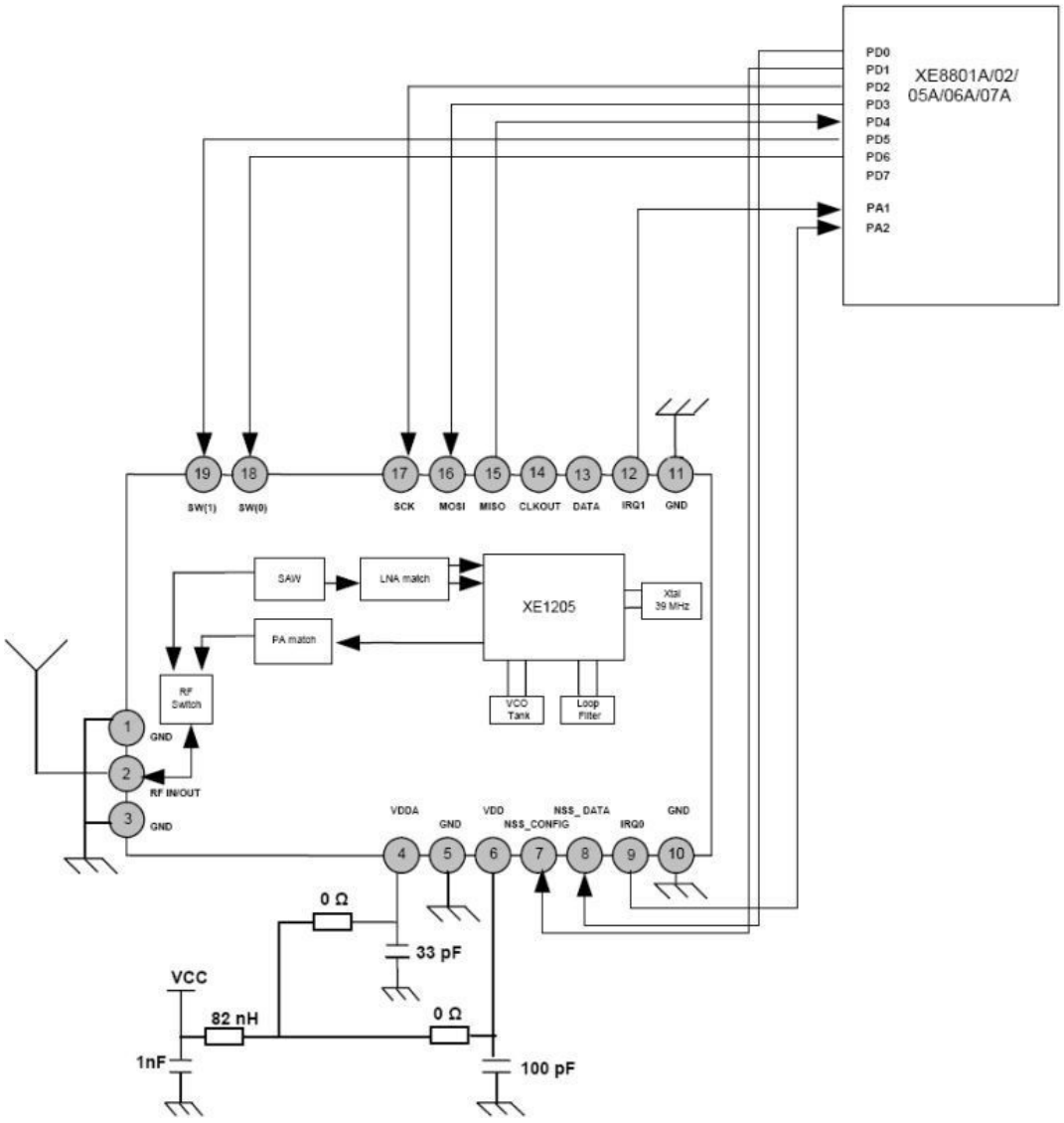
By default, the serial control interface is used for configuration. It is also possible to change between the four modes (sleep, stand-by, receive, transmit) by using the two-bit signal SW(1:0). This option is enabled by setting the bit MCParam_Select_mode to '1' in the configuration register.
If MCParam_Select_mode is low, the modes are defined by the register through the SPI_CONFIG interface and SW(1:0) may be used as an output to control, for example, an antenna switch.

MCParam_Select_mode **Bit 5, Address 0**	**SWITCH (pin)** **SW(1:0)**	**MCParam_chip_mode** **Bit 7-6, Address 0**
0	Set in Output sleep mode -> SW(1:0) = "00" receiver mode -> SW(1:0) = "01" transmitter mode -> SW(1:0) = "10" stand-by mode -> SW(1:0) = "00"	00 -> sleep mode 01 -> receive mode 10 -> transmit mode 11 -> stand-by mode
1	SW(1:0) = 00 -> sleep mode SW(1:0) = 01 -> receive mode SW(1:0) = 10 -> transmit mode SW(1:0) = 11 -> stand-by mode	x

For more information about the modes of operation, please refer to the XE1205 Datasheet on the Semtech website http://www.semtech.com .

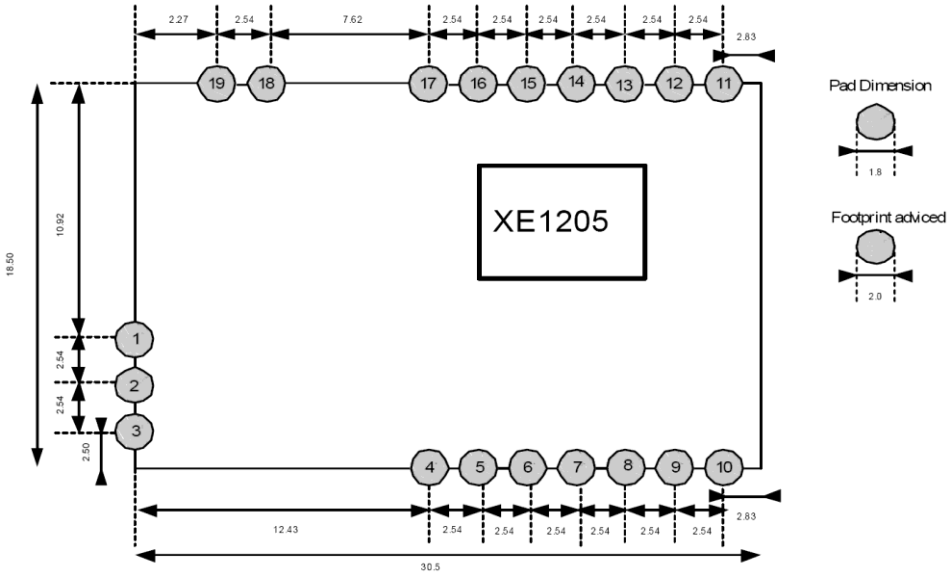
8. TYPICAL APPLICATION

The schematic below shows the DP1205 interfaced with a Semtech microcontroller XE8801A/02/05A/6A/07A and the XE1205 used in buffered mode.



9. MECHANICAL DIMENSIONS

The following diagram shows the physical footprint and dimensions of the DP1205 drop-in module, which should be implemented on the mother board.



Version	Create Date:	Creater	Changes
01	21.09.10	Hermann	Create new Datasheet
02	18.10.12	Hermann	Update

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