Features

- 8-channel, 24-bit simultaneous sampling analog-to-digital converter
- Bipolar (±1.65 V) or unipolar (3.3 V) supplies
- Programmable gain amplifier (PGA) per channel (gains of 1, 2, 4,and 8)
- Up to 16 kSPS output data rate (ODR) per channel
- Single-ended or true differential inputs
- Low resolution successive approximation (SAR) ADC for system

Application

- Circuit breaker
- General data collection
- Medical electronics
- Industrial control system
- Instrument measurement

Description

The CBM08AD24Q is an 8-channel, simultaneous sampling ADC. There are eight full Σ-Δ ADCs on chip. The CBM08AD24Q provides an ultra-low input current to allow direct sensor connection. Each input channel has a programmable gain stage allowing gains of 1, 2, 4, and 8 to map lower amplitude sensor outputs into the full-scale ADC input range, maximizing the dynamic range of the signal chain.The CBM08AD24Q accepts VREF from 1 V up to 3.6 V. The analog inputs accept unipolar (0 V to VREF/GAIN) or true bipolar (±VREF/ GAIN/2 V) analog input signals with 3.3 V or ±1.65 V analog supply voltages. The analog inputs can be configured to accept true differential, pseudo differential, or single-ended signals to match different sensor output configurations.The ADC data output interface is dedicated to transmitting the ADC conversion results from the CBM08AD24Q to the processor. The SPI interface is used to write to and read from the CBM08AD24Q configuration registers and for the control and reading of data from the SAR ADC. The SPI interface can also be configured to output the Σ-Δ conversion data. The CBM08AD24Q includes a 12-bit SAR ADC. This ADC can be used for CBM08AD24Q diagnostics without having to decommission one of the Σ-Δ ADC channels dedicated to system measurement functions. With the use of an external multiplexer, which can be controlled through the three general-purpose inputs/outputs pins (GPIOs), and signal conditioning, the SAR ADC can be used to validate the Σ-Δ ADC measurements in applications where functional safety is required.

In addition, the CBM08AD24Q SAR ADC includes an internal multiplexer to sense internal nodes.The product offers two working modes: high-resolution mode and low-power mode. The high-resolution mode provides a higher dynamic range, while the low-power mode reduces power consumption at lower dynamic range specifications.

Catalog

Block Diagram

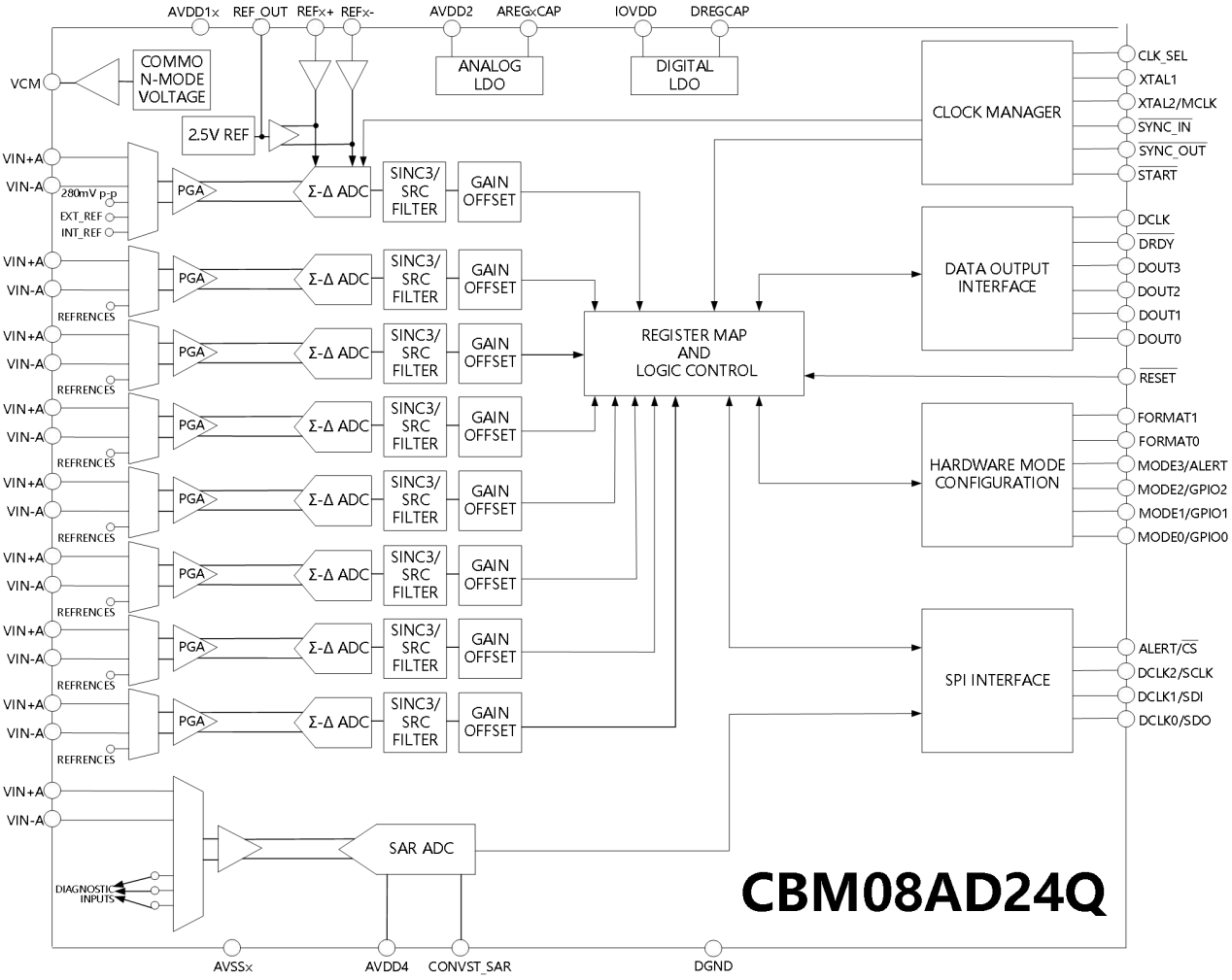

Figure 1. Block Diagram

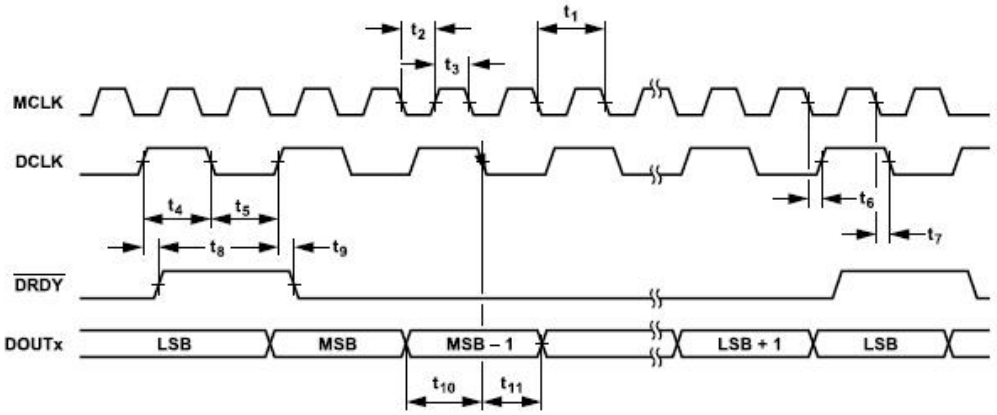

Figure 2. Product Data Interface Sequence Diagram

Table 1: timing

Prameter	Description[1]	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	MCLK frequency	50 : 50	0.655		8.192	MHz
t_2	MCLK low time		60			ns
t_3	MCLK high time		60			ns
t_4	DCLKx high time	MCLK/2		122		ns
t_5	DCLKx low time	MCLK/2		122		ns
t_6	MCLK rising edge to DCLK rising edge			15		ns
t_7	MCLK falling edge to DCLK rising edge			15		ns
t_8	DCLKx rising edge to DRDY rising edge			5		ns
t_9	DCLKx rising edge to DRDY falling edge					ns
t_{10}	DOUTx setup time		20	5		ns
t_{11}	DOUTx hold time		20			ns

[1]All input signals are specified with tR = tF = 1 ns/V (10% to 90% of IOVDD) and timed from a voltage level of (VIL + VIH)/2.

Product Outline Dimensions

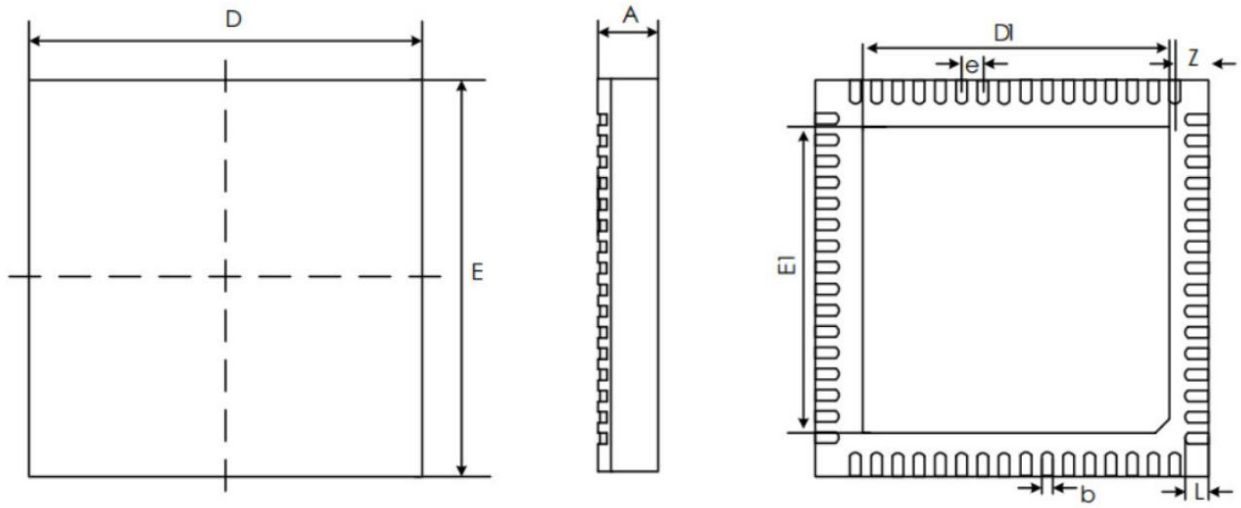

Figure 3. Package Outline Drawing

Unit:mm

Symbol	Value			Symbol	Value		
	Min	Typ	Max		Min	Typ	Max
A	0.60	--	1.00	D	8.80	--	9.20
b	0.20	--	0.30	E	8.80	--	9.20
e	--	0.50	--	E1	7.40	--	7.80
L	0.30	--	0.50	D1	7.40	--	7.80
Z	--	--	0.95				

Pin Description

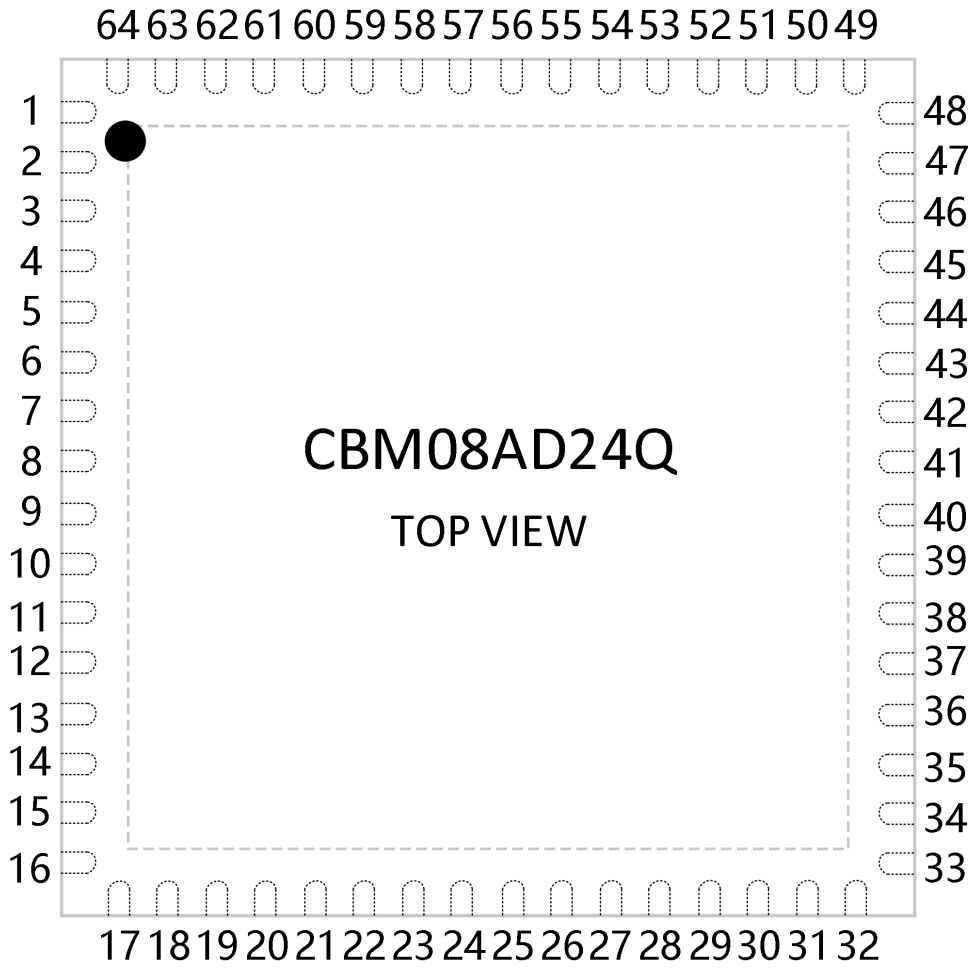

Figure 4.Pin Assignment

Pin No.	Mnemonic	Name	Pin No.	Symbol	Name
1	AINO-	Analog input 0(Negative)	33	$\overline{\text{START}}$	Synchronization Pulse
2	AINO+	Analog input 0(Positive)	34	$\overline{\text{SYNC\_OUT}}$	Synchronization Signal
3	AIN1-	Analog input 1(Negative)	35	$\overline{\text{SYNC\_IN}}$	Reset for the Internal Digital Block and Synchronize for Multiple Devices
4	AIN1+	Analog input 1(Positive)	36	$\overline{\text{RESET}}$	Asynchronous Reset signal
5	GNDA	Analog ground	37	AIN7+	Analog Input Channel 7, Positive
6	VCC1	Analog supply 1	38	AIN7-	Analog Input Channel 7,

					Negative
7	REF1-	Negative Reference Input 1 for Channel 0 to Channel 3,	39	AIN6+	Analog Input Channel 6, Positive
8	REF1+	Positive Reference Input 1 for Channel 0 to Channel 3	40	AIN6-	Analog Input Channel 6, Negative
9	AIN2-	Analog Input Channel 2, Negative.	41	REF2+	Positive Reference Input 2 for Channel 4 to Channel 7
10	AIN2+	Analog Input Channel 2, Positive.	42	REF2	Negative Reference Input 2 for Channel 4 to Channel 7
11	AIN3-	Analog Input Channel 3, Negative.	43	VCC1	Analog Supply 1
12	AIN3+	Analog Input Channel 3, Positive.	44	GNDA	Analog ground
13	MODE0	Mode 0 Input Pin	45	AIN5+	Analog Input Channel 5, Positive
Pin No.	**Mnemonic**	**Name**	**Pin No.**	**Symbol**	**Name**
14	MODE1	Mode 1 Input Pin	46	AIN5-	Analog Input Channel 5, Negative
15	MODE2	Mode 2 Input Pin	47	AIN4+	Analog Input Channel 4, Positive
16	MODE3	Mode 3 Input Pin	48	AIN4-	Analog Input Channel 4, Negative
17	CONVST _SAR	Start signal for SAR conversion	49	REF_OUT	Reference Output
18	ALERT/ $\overline{CS}$	Alarm signal/SPI chip selection signal	50	GNDA	Analog ground
19	DCLK2/SCLK	Frequency selection signal 2/SPI clock signal	51	AREG2CAP	Analog LDO Output 2
20	DCLK1/SDI	Frequency selection signal 1/SPI data input	52	VCC2	Analog Supply 2
21	DCLKO/SDO	Frequency selection signal 0/SPI data output	53	GNDA	Analog ground
22	GNDD	Digital ground	54	FORMAT1	Output Data Frame 1

23	DREGCAP	Digital LDO Output	55	FORMAT0	Output Data Frame 0
24	VIODD	Digital supply	56	CLK_SEL	Select Clock Source
25	DOUT3	Data Output Pin 3	57	VCM	Common-Mode Voltage Output
26	DOUT2	Data Output Pin 2	58	VCC2	Analog Supply 2
27	DOUT1	Data Output Pin 1	59	AREG1CAP	Analog LDO Output 1
28	DOUT0	Data Output Pin 0	60	GNDA	Analog ground
29	DCLK	Data Output Clock	61	GNDA	Analog ground
30	$\overline{\text{DCLK}}$	Data Output Ready Pin	62	VCC4	Analog Supply 4
31	XTAL1	Crystal 1 Input Connection	63	AUXAIN+	Positive SAR Analog Input Channel
32	XTAL2/MCLK	Crystal 2 Input Connection/CMOS Clock (MCLK).	64	AUXAIN-	Negative SAR Analog Input Channel

Recommended Operation Conditions

- Operating frequency (f_{CLK}): ≤ 8192KHz
- Power supply voltage (V_{CC1}): 3.0V~3.6V
- Power supply voltage (V_{CC2}): 3.0V~3.6V
- Power supply voltage (V_{CC4}): 3.0V~3.6V
- Power supply voltage (V_{IOVDD}): 1.8V~3.6V
- Operating environment temperature (TA): -40 ℃~85 ℃

Absolute Maximum Ratings

- Power supply voltage (V_{CC1}): 3.96V
- Power supply voltage (V_{CC2}): 3.96V
- Power supply voltage (V_{CC4}): 3.96V
- Power supply voltage (V_{IOVDD}): 3.96V
- Storage temperature (T_{tsg}): -65 ℃~150 ℃
- Junction temperature (T_J): 150 ℃

Specifications

The electrical characteristics after packaging are shown in the table. Unless otherwise specified, the test conditions are as follows: V_{CC1}=V_{CC2}=V_{CC4}=3.3V, V_{IODD}=3.3V, GND_A=GND_D=OV, M_{CLK}=8192KHz (-40℃ ≤ T_A≤ 85℃).

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
DC parameters						
Resolution	RES		24			bits
Number of channels	L		8			channels
Offset Error	E_O	T_A=25℃	-100	-	100	uV
Gain Error	E_G	T_A=25℃	-1	±0.2	1	%FS
Integral nonlinear error	E_L	T_A=25℃	-15	-	15	ppm
Reference output voltage	V_{REF}	T_A=25℃	2.4	2.5	2.6	V
Power supply current	I		-	60	152	mA
power dissipation	P_D		-	200	500	mW
AC parameters						
Signal to Noise Ratio	SNR		100	106	-	dB
Signal-to-noise distortion ratio	SINAD		95		-	dB
Total harmonic distortion	SFDR				-100	dB
SFDR	THD		90			dB
Digital parameters						
Input high voltage	V_{IH}		0.7×V_{IODD}			V
Input low voltage	V_{IL}				0.4	V
Output high voltage	V_{OH}		0.7×V_{IODD}			V

Output low voltage	V_{OL}				0.4	V
Switch parameters						
Output data rate	ODR		16	-	-	KSPS

Typical Performance Characteristics

1,Dynamic parameter test results

Test conditions:

(1) Sampling rate: f_{CLK}=8192KHz; Input signal frequency: f_{IN}=60Hz;T_A=25℃

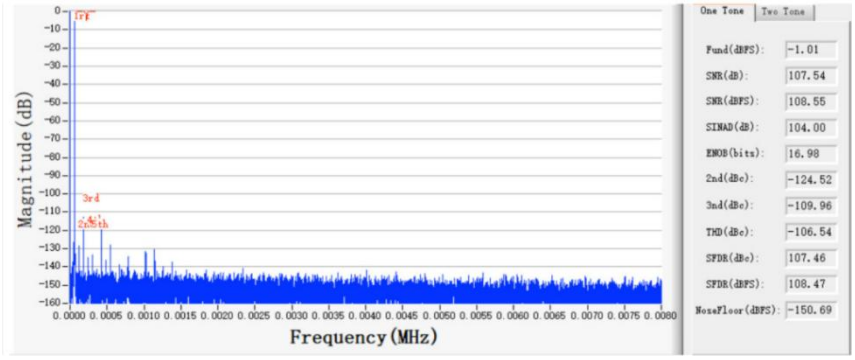

Figure 5. Low frequency and room temperature test results of dynamic characteristics

(2) Sampling rate: f_{CLK}=8192KHz; Input signal frequency: f_{IN}=1KHz; T_A=25℃

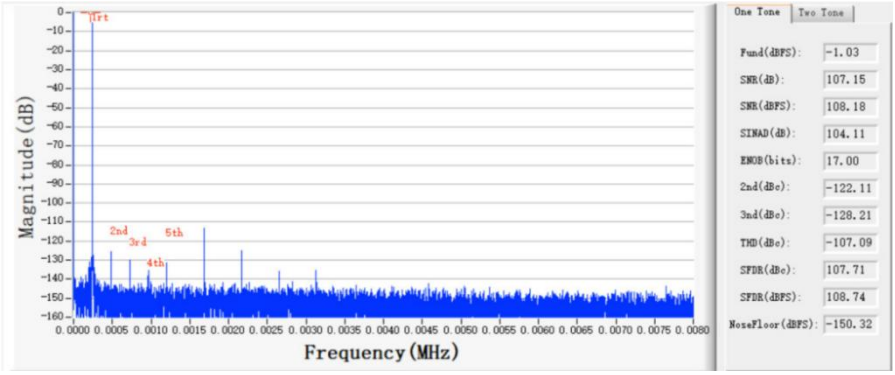

Figure 6. Low frequency and room temperature test results of dynamic characteristics

2,Static parameter test results

Test conditions: Sampling rate: f_{CLK}=8192KHz; T_A=25℃

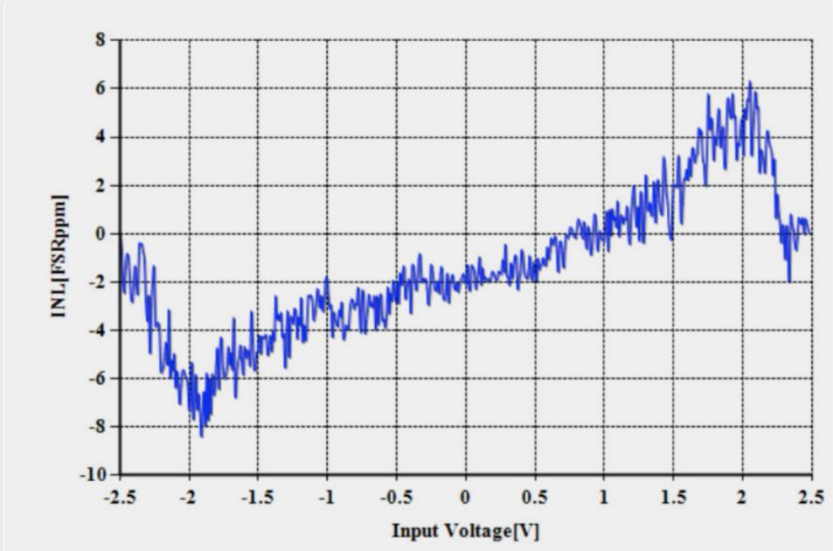

Figure 7. Static indicator test results

Typical Applications

Analog Input

CBM08AD24Q can operate in bipolar or unipolar modes, supporting true differential, pseudo differential, and single ended input signals, as shown in the figure 8.

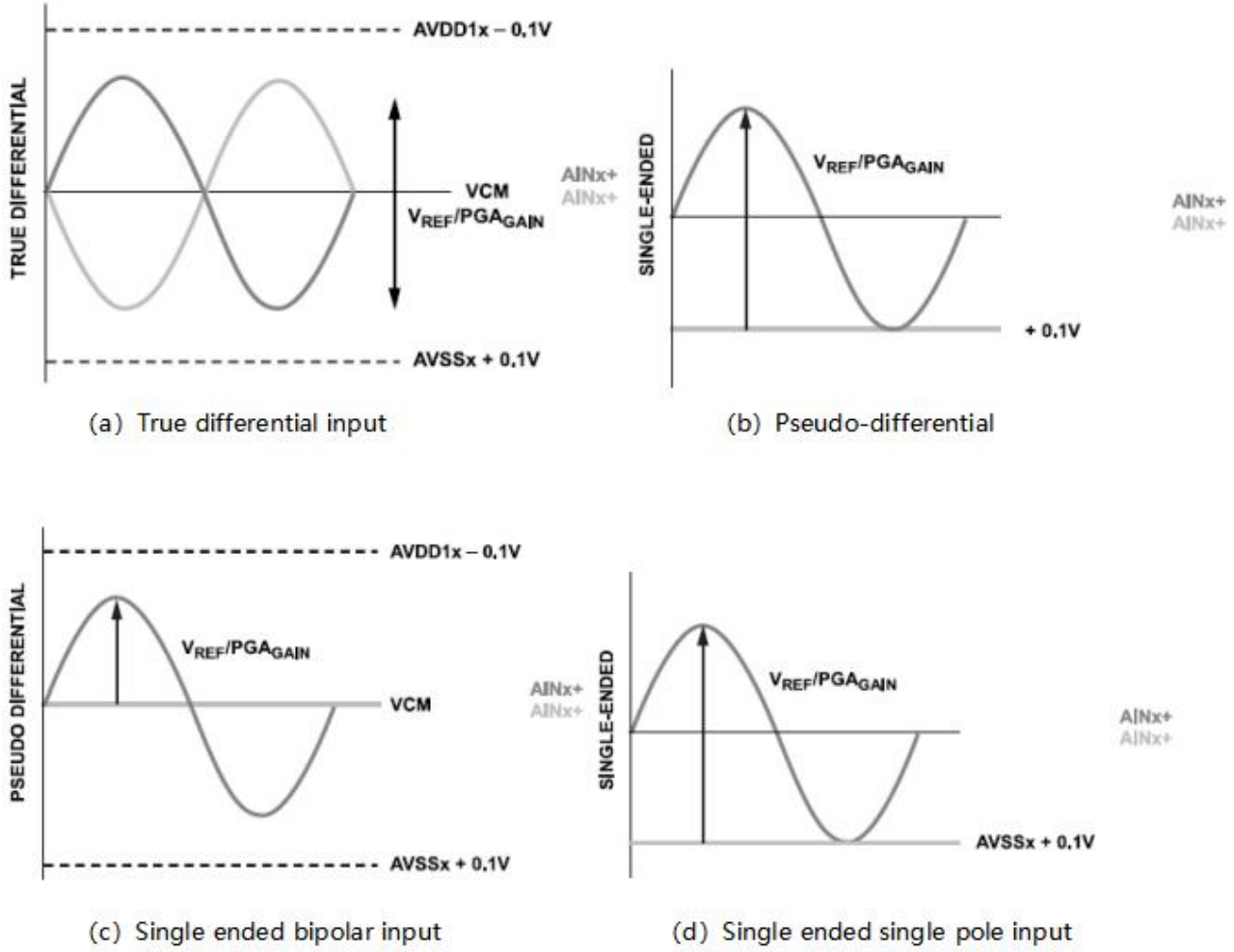

Figure 8. ADC input signal configuration

The input signal common mode is not limited, but keep the absolute input signal voltage on any AINx± pin between AVSSx + 100 mV and AVDD1x −100 mV; otherwise, the input signal linearity degrades and, if the signal voltage exceeds the absolute maximum signal rating, damages the device.

Core Signal Chain

Each Σ-Δ ADC channel on the CBM08AD24Q has an identical signal path from the analog input pins to the digital output pins. Prior to each Σ-Δ ADC, a PGA maps sensor outputs into the ADC inputs, providing low input current in dc (±4 nA, input current, and ±1.5 nA differential input current), an 8 pF input capacitance in ac, and configurable gains of 1, 2, 4, and 8. Each ADC channel has its own Σ-Δ modulator, which

oversamples the analog input and passes the digital representation to the digital filter block. The data is filtered, scaled for gain and offset, and is then output on the data interface.To minimize power consumption, individually disable the channels.

Capacitive PGA

Each Σ-Δ ADC has a dedicated PGA, offering gain ranges of 1, 2,4, and 8. This PGA reduces the need for an external input buffer and allows the user to amplify small sensor signals to use the full dynamic range of the CBM08AD24Q.The PGA maximize the signal chain dynamic range for small sensor output signals.The CBM08AD24Q uses chopping of the PGA to minimize offset and offset drift in the input amplifier, reducing the 1/f noise as well.For the CBM08AD24Q, the chopping frequency is set to 64 kHz for high resolution mode, and 16 kHz for low power mode..To minimize intermodulation effects that may cause image in the band of interest, it is recommended to limit the input signal bandwidth to 2/3 of the chop frequency.The capacitive PGA common-mode voltage does not depend on the gain, and can be any value as long as the input signal voltage is within AVSSx + 100 mV to AVDD1x − 100 mV.

Internal Reference and Reference Buffers

The CBM08AD24Q integrates a 2.5 V, 10 ppm/°C typical, voltage reference that is disabled at power-up. The buffered reference is available at Pin 49 and offers up to 10 mA of continuous current. A 100 nF capacitor is required if the reference is enabled.

The reference buffers can be operated in three different modes:buffer enabled mode, buffer bypassed mode, and buffer precharged mode.In buffer enabled mode, the buffer is fully enabled, minimizing the current requirements from the external references. Note that the buffer output voltage headroom is ±100 mV from the rails.In buffer bypassed mode, the external reference is directly connected to the ADC reference capacitors; the reference must provide enough current to correctly charge the internal ADC reference capacitors. In this mode of operation, a degradation in crosstalk is expected because the ADC channels are not isolated from each other.

Buffer precharged (pre-Q) mode is the default operation mode. It is a hybrid mode where the internal reference buffers are connected during the initial acquisition time to precharge the internal ADC reference capacitors. During the final phase of the acquisition, the reference is connected directly to the ADC capacitors. This mode has some benefits compared to the buffer enabled and buffer bypassed modes. In buffer precharged mode, the reference current requirements are minimized compared to buffer bypassed mode the noise contribution from the internal reference buffers is removed(compared to buffer enabled mode).In buffer precharged mode, the headroom/footroom of the buffer reference is not applicable because the reference sets the final voltage in the ADC reference capacitors.

Clocking and Sampling

The CBM08AD24Q includes eight Σ-Δ ADC cores. Each ADC receives the same master clock signal. The CBM08AD24Q requires a maximum external MCLK frequency of 8192 kHz for high resolution mode and 4096 kHz for low power mode. The MCLK is internally divided by 4 in high resolution mode and by 8 in low power mode to produce the modulator MCLK (MOD_MCLK) signal used as the modulator sampling clock for the ADCs. The MCLK can be decreased to accommodate lower ODRs if the minimum ODR selected by the SINC filter is not low enough. If the external clock is lower than 250 kHz, set the CLK_QUAL_DIS bit (in SPI control mode only).

Digital Filtering

The CBM08AD24Q offers a low latency sinc3 filter. Most precision Σ-Δ ADCs use sinc3 filters because the sinc3 filter offers a low latency path for applications requiring low bandwidth signals, for example,in control loops or where application specific post processing is required. The digital filter adds notches at multiples of the sampling frequency.The digital filter implements three main notches, one at the maximum ODR (16 kHz or 8 kHz, depending on the power mode) and another two at the ODR frequency selected to stop noise aliasing into the pass band.

SPI Control

The second option for control and monitoring the CBM08AD24Q is via the SPI interface. This option allows access to the full functionality on the CBM08AD24Q, including access to the SAR converter, phase synchronization, offset and gain adjustment, diagnostics and the SRC. To use the SPI control, set the FORMAT0 and FORMAT1 pins to logic high.In this mode, the SPI interface can also be used to read the Σ-Δ conversation data by setting the SPI_SLAVEMODE_EN bit.

Register Summary

Reg.	Name	Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset	R/W
0x000	CH0_CONFIG	[7:0]	CH0_GAIN		CH0_REF_MONITOR	CH0_RX	RESERVED				0x00	/WR
0x001	CH1_CONFIG	[7:0]	CH1_GAIN		CH1_REF_MONITOR	CH1_RX	RESERVED				0x00	R/W
0x002	CH2_CONFIG	[7:0]	CH2_GAIN		CH2_REF_MONITOR	CH2_RX	RESERVED				0x00	R/W
0x003	CH3_CONFIG	[7:0]	CH3_GAIN		CH3_REF_MONITOR	CH3_RX	RESERVED				0x00	R/W
0x004	CH4_CONFIG	[7:0]	CH4_GAIN		CH4_REF_MONITOR	CH4_RX	RESERVED				0x00	R/W
0x005	CH5_CONFIG	[7:0]	CH5_GAIN		CH5_REF_MONITOR	CH5_RX	RESERVED				0x00	R/W
0x006	CH6_CONFIG	[7:0]	CH6_GAIN		CH6_REF_MONITOR	CH6_RX	RESERVED				0x00	R/W
0x007	CH7_CONFIG	[7:0]	CH7_GAIN		CH7_REF_MONITOR	CH7_RX	RESERVED				0x00	R/W

0x008	CH_DISABLE	[7:0]	CH7_ DISABLE	CH6_ DISABLE	CH5_DISABLE	CH4_ DISABLE	CH3_ DISABLE	CH2_ DISABLE	CH1_ DISABLE	CH0_ DISABLE	0x00	R/W
0x009	CH0_SYNC_ OFFSET	[7:0]	CH0_SYNC_OFFSET								0x00	R/W
0x00A	CH1_SYNC_ OFFSET	[7:0]	CH1_SYNC_OFFSET								0x00	R/W
0x00B	CH2_SYNC_ OFFSET	[7:0]	CH2_SYNC_OFFSET								0x00	R/W
0x00C	CH3_SYNC_ OFFSET	[7:0]	CH3_SYNC_OFFSET								0x00	R/W
0x00D	CH4_SYNC_ OFFSET	[7:0]	CH4_SYNC_OFFSET								0x00	R/W
0x00E	CH5_SYNC_ OFFSET	[7:0]	CH5_SYNC_OFFSET								0x00	R/W

Reg.	**Name**	**Bits**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Reset**	**R/W**
0x00F	CH6_SYNC_ OFFSET	[7:0]	CH6_SYNC_OFFSET								0x00	R/W
0x010	CH7_SYNC_ OFFSET	[7:0]	CH7_SYNC_OFFSET								0x00	R/W
0x011	GENERAL_ USER CONFIG_1	[7:0]	ALL_ CH_DIS_ MCLK_EN	POWER_ MODE	PDB_VCM	PDB_ REFOUT_ BUF	PDB_SAR	PDB_ RC_OSC	SOFT_RESET		0x24	R/W
0x012	GENERAL_ USER CONFIG_2	[7:0]	RESERVED		SAR_DIAG_MODE_EN	SDO_DRIVE_STR		DOUT_DRIVE_STR		SPI_SYNC	0x09	R/W
0x013	GENERAL_ USER CONFIG_3	[7:0]	CONVST_ DEGLITCH_ DIS		RESERVED	SPI_SLAVE_ MODE_EN	RESERVED			CLK_ QUAL_DI S	0x80	R/W
0x014	DOUT_FORMAT	[7:0]	DOUT_FORMAT		DOUT_HEADER_FORMA T	RESERVED				RESERVE D	0x20	R/W
0x015	ADC_MUX_ CONFIG	[7:0]	REF_MUX_ CTRL		MTR_MUX_CTRL				RESERVED		0x00	R/W

0x016	GLOBAL_MUX_CONFIG	[7:0]	GLOBAL MUX CTRL						RESERVED			0x00	R/W
0x017	GPIO_CONFIG	[7:0]	RESERVED						GPIO_OP_EN			0x00	R/W
0x018	GPIO_DATA	[7:0]	RESERVED						IO_WRITE_DATA			0x00	R/W
0x019	BUFFER_CONFIG_1	[7:0]	RESERVED					REF_BUF_POS_EN	REF_BUF_NEG_EN	RESERVED		0x38	R/W
0x01A	BUFFER_CONFIG_2	[7:0]	REF_BUFP_PREQ	REF_BUFN_PREQ	RESERVED					PDB_ALDO1_OVRDRV	PDB_ALDO2_OVRDRV	PDB_DLDO_OVRDRU	0xC0	R/W
0x01C	CH0_OFFSET_UPPER_BYTE	[7:0]	CH0_OFFSET_ALL[23:16]									0x00	R/W
0x01D	CH0_OFFSET_MID_BYTE	[7:0]	CH0_OFFSET_ALL[15:8]									0x00	R/W
0x01E	CH0_OFFSET_LOWER_BYTE	[7:0]	CH0_OFFSET_ALL[7:0]									0x00	R/W
0x01F	CH0_GAIN_UPPER_BYTE	[7:0]	CH0_GAIN_ALL[23:16]									0x00	R/W
0x020	CH0_GAIN_MID_BYTE	[7:0]	CH0_GAIN_ALL[15:8]									0x00	R/W
0x021	CH0_GAIN_LOWER_BYTE	[7:0]	CH0_GAIN_ALL[7:0]									0x00	R/W
0x022	CH1_OFFSET_UPPER_BYTE	[7:0]	CH1_OFFSET_ALL[23:16]									0x00	R/W
0x023	CH1_OFFSET_MID_BYTE	[7:0]	CH1_OFFSET_ALL[15:8]									0x00	R/W
0x024	CH1_OFFSET_LOWER_BYTE	[7:0]	CH1_OFFSET_ALL[7:0]									0x00	R/W
0x025	CH1_GAIN_UPPER_BYTE	[7:0]	CH1_GAIN_ALL[23:16]									0x00	R/W
0x026	CH1_GAIN_MID_BYTE	[7:0]	CH1_GAIN_ALL[15:8]									0x00	R/W

0x027	CH1_GAIN_ LOWER_BYTE	[7:0]	CH1_GAIN_ALL[7:0]	0x00	R/W

Reg.	Name	Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset	R/W
0x028	CH2_OFFSET_ UPPER_BYTE	[7:0]	CH2_OFFSET_ALL[23:16]								0x00	R/W
0x029	CH2_OFFSET_ MID_BYTE	[7:0]	CH2_OFFSET_ALL[15:8]								0x00	R/W
0x02A	CH2_OFFSET_ LOWER_BYTE	[7:0]	CH2_OFFSET_ALL[7:0]								0x00	R/W
0x02B	CH2_GAIN_ UPPER_BYTE	[7:0]	CH2_GAIN_ALL[23:16]								0x00	R/W
0x02C	CH2_GAIN_ MID_BYTE	[7:0]	CH2_GAIN_ALL[15:8]								0x00	R/W
0x02D	CH2_GAIN_ LOWER_BYTE	[7:0]	CH2_GAIN_ALL[7:0]								0x00	R/W
0x02E	CH3_OFFSET_ UPPER_BYTE	[7:0]	CH3_OFFSET_ALL[23:16]								0x00	R/W
0x02F	CH3_OFFSET_ MID_BYTE	[7:0]	CH3_OFFSET_ALL[15:8]								0x00	R/W
0x030	CH3_OFFSET_ LOWER_BYTE	[7:0]	CH3_OFFSET_ALL[7:0]								0x00	R/W
0x031	CH3_GAIN_ UPPER_BYTE	[7:0]	CH3_GAIN_ALL[23:16]								0x00	R/W
0x032	CH3_GAIN_ MID_BYTE	[7:0]	CH3_GAIN_ALL[15:8]								0x00	R/W
0x033	CH3_GAIN_ LOWER_BYTE	[7:0]	CH3_GAIN_ALL[7:0]								0x00	R/W
0x034	CH4_OFFSET_ UPPER_BYTE	[7:0]	CH4_OFFSET_ALL[23:16]								0x00	R/W
0x035	CH4_OFFSET_ MID_BYTE	[7:0]	CH4_OFFSET_ALL[15:8]								0x00	R/W

0x036	CH4_OFFSET_ LOWER_BYTE	[7:0]	CH4_OFFSET_ALL[7:0]							0x00	R/W
0x037	CH4_GAIN_ UPPER_BYTE	[7:0]	CH4_GAIN_ALL[23:16]							0x00	R/W
0x038	CH4_GAIN_ MID_BYTE	[7:0]	CH4_GAIN_ALL[15:8]							0x00	R/W
0x039	CH4_GAIN_ LOWER_BYTE	[7:0]	CH4_GAIN_ALL[7:0]							0x00	R/W
0x03A	CH5_OFFSET_ UPPER_BYTE	[7:0]	CH5_OFFSET_ALL[23:16]							0x00	R/W
0x03B	CH5_OFFSET_ MID_BYTE	[7:0]	CH5_OFFSET_ALL[15:8]							0x00	R/W
0x03C	CH5_OFFSET_ LOWER_BYTE	[7:0]	CH5_OFFSET_ALL[7:0]							0x00	R/W
0x03D	CH5_GAIN_ UPPER_BYTE	[7:0]	CH5_GAIN_ALL[23:16]							0x00	R/W
0x03E	CH5_GAIN_ MID_BYTE	[7:0]	CH5_GAIN_ALL[15:8]							0x00	R/W
0x03F	CH5_GAIN_ LOWER_BYTE	[7:0]	CH5_GAIN_ALL[7:0]							0x00	R/W
0x040	CH6_OFFSET_ UPPER_BYTE	[7:0]	CH6_OFFSET_ALL[23:16]							0x00	R/W
0x041	CH6_OFFSET_ MID_BYTE	[7:0]	CH6_OFFSET_ALL[15:8]							0x00	R/W
Reg.	**Name**	**Bits**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Reset**	**R/W**
0x042	CH6_OFFSET_ LOWER_BYTE	[7:0]	CH6_OFFSET_ALL[7:0]								0x00	R/W
0x043	CH6_GAIN_ UPPER_BYTE	[7:0]	CH6_GAIN_ALL[23:16]								0x00	R/W
0x044	CH6_GAIN_ MID_BYTE	[7:0]	CH6_GAIN_ALL[15:8]								0x00	R/W
0x045	CH6_GAIN_ LOWER_BYTE	[7:0]	CH6_GAIN_ALL[7:0]								0x00	R/W

0x046	CH7_OFFSET_ UPPER_BYTE	[7:0]	CH7_OFFSET_ALL[23:16]							0x00	R/W
0x047	CH7_OFFSET_ MID_BYTE	[7:0]	CH7_OFFSET_ALL[15:8]							0x00	R/W
0x048	CH7_OFFSET_ LOWER_BYTE	[7:0]	CH7_OFFSET_ALL[7:0]							0x00	R/W
0x049	CH7_GAIN_ UPPER_BYTE	[7:0]	CH7_GAIN_ALL[23:16]							0x00	R/W
0x04A	CH7_GAIN_ MID_BYTE	[7:0]	CH7_GAIN_ALL[15:8]							0x00	R/W
0x04B	CH7_GAIN_ LOWER_BYTE	[7:0]	CH7_GAIN_ALL[7:0]							0x00	R/W
0x04C	CH0_ERR_REG	[7:0]	RESERVED		CH0_ERR_ AINM_UV	CH0_ERR_ AINM_OV	CH0_ERR_ AINP_UV	CH0_ERR_ AINP_OV	CHO_ERR _REF_DET	0x00	R
0x04D	CH1_ERR_REG	[7:0]	RESERVED		CH1_ERR_ AINM_UV	CH1_ERR_ AINM_OV	CH1_ERR_ AINP_UV	CH1_ERR_ AINP_OV	CH1_ERR_ REF_DET	0x00	R
0x04E	CH2_ERR_REG	[7:0]	RESERVED		CH2_ERR_ AINM_UV	CH2_ERR_ AINM_OV	CH2_ERR_ AINP_UV	CH2_ERR_ AINP_OV	CH2_ERR_ REF_DET	0x00	R
0x04F	CH3_ERR_REG	[7:0]	RESERVED		CH3_ERR_ AINM_UV	CH3_ERR_ AINM_OV	CH3_ERR_ AINP_UV	CH3_ERR_ AINP_OV	CH3_ERR_ REF_DET	0x00	R
0x050	CH4_ERR_REG	[7:0]	RESERVED		CH4_ERR_ AINM_UV	CH4_ERR_ AINM_OV	CH4_ERR_ AINP_UV	CH4_ERR_ AINP_OV	CH4_ERR_ REF_DET	0x00	R
0x051	CH5_ERR_REG	[7:0]	RESERVED		CH5_ERR_ AINM_UV	CH5_ERR_ AINM_OV	CH5_ERR_ AINP_UV	CH5_ERR_ AINP_OV	CH5_ERR_ REF_DET	0x00	R
0x052	CH6_ERR_REG	[7:0]	RESERVED		CH6_ERR_ AINM_UV	CH6_ERR_ AINM_OV	CH6_ERR_ AINP_UV	CH6_ERR_ AINP_OV	CH6_ERR_ REF_DET	0x00	R
0x053	CH6_ERR_REG	[7:0]	RESERVED		CH7_ERR_ AINM_UV	CH7_ERR_ AINM_OV	CH7_ERR_ AINP_UV	CH7_ERR_ AINP_OV	CH7_ERR_ REF_DET	0x00	R
0x054	CH0_1_SAT_ERR	[7:0]	RESERVED	CH1_ERR_MOD_SAT	CH1_ERR_F ILTER_ SAT	CH1_ERR_ OUT_PUT_ SAT	CH0_ERR_ MOD_SAT	CH0_ERR_F ILTER_ SAT	CH0_ERR_ OUTPUT_ SAT	0x00	R

0x055	CH2_3_SAT_ERR	[7:0]	RESERVED		CH3_ERR_MOD_SAT	CH3_ERR_FILTER_SAT	CH3_ERR_OUT_PUT_SAT	CH2_ERR_MOD_SAT	CH2_ERR_FILTER_SAT	CH2_ERR_OUTPUT_SAT	0x00	R
0x056	CH4_5_SAT_ERR	[7:0]	RESERVED		CH5_ERR_MOD_SAT	CH5_ERR_FILTER_SAT	CH5_ERR_OUT_PUT_SAT	CH4_ERR_MOD_SAT	CH4_ERR_FILTER_SAT	CH4_ERR_OUTPUT_SAT	0x00	R
0x057	CH6_7_SAT_ERR	[7:0]	RESERVED		CH7_ERR_MOD_SAT	CH7_ERR_FILTER_SAT	CH7_ERR_OUT_PUT_SAT	CH6_ERR_MOD_SAT	CH6_ERR_FILTER_SAT	CH6_ERR_OUTPUT_SAT	0x00	R
0x058	CHX_ERR_REG_EN	[7:0]	OUTPUT_SAT_TEST_EN	FILTER_SAT_TEST_EN	MOD_SAT_TEST_EN	AINM_UV_TEST_EN	AINM_OV_TEST_EN	AINP_UV_TEST_EN	AINP_OV_TEST_EN	REF_DET_TEST_EN	0xFE	R/W
0x059	GEN_ERR_REG_1	[7:0]	RESERVED		MEMMAP_CRC_ERR	ROM_CRC_ERR	SPI_CLK_COUNT_ERR	SPI_INVALID_READ_ERR	SPI_INVALID_WRITE_ERR	SPI_CRC_ERR	0x00	R
0x05A	GEN_ERR_REG_1_EN	[7:0]	RESERVED		MEMMAP_CRC_TEST_ERR	ROM_CRC_TEST_ERR	SPI_CLK_COUNT_TEST_EN	SPI_INVALID_READ_TEST_EN	SPI_INVALID_WRITE_TEST_EN	SPI_CRC_TEST_EN	0x3E	R/W

Reg.	**Name**	**Bits**	**Bit7**	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**	**Reset**	**R/W**
0x05B	GEN_ERR_REG_2	[7:0]	RESERVED		RESET_DETECTED	EXT_MCLK_SWITCH_ERR	RESERVED	ALDO1_PSM_ERR	ALDO2_PSM_ERR	DLDO_PSM_ERR	0x00	R
0x05C	GEN_ERR_REG_2_EN	[7:0]	RESERVED		RESET_DETECT_EN	RESERVED					0x3C	R/W
0x05D		[7:0]	RESERVED			ERR_LOC_CH4	ERR_LOC_CH3	ERR_LOC_CH2	ERR_LOC_CH1	ERR_LOC_CH0	0x00	R
0x05E		[7:0]	RESERVED			ERR_LOC_GEN2	ERR_LOC_CEN1	ERR_LOC_CH7	ERR_LOC_CH6	ERR_LOC_CH5	0x00	R
0x05F		[7:0]	RESERVED			INIT_COMPLETE	ERR_LOC_SAT_CH6_7	ERR_LOC_SAT_CH4_5	ERR_LOC_SAT_CH2_3	ERR_LOC_SAT_CH0_1	0x00	R
0x060	SRC_N_MSB	[7:0]	RESERVED				SRC_N_ALL[11:8]				0x00	R/W

0x061	SRC_N_LSB	[7:0]	SRC_N_ALL[7:0]			0x80	R/W
0x062	SRC_IF_MSB	[7:0]	SRC_IF_ALL[15:8]			0x00	R/W
0x063	SRC_IF_LSB	[7:0]	SRC_IF_ALL[7:0]			0x00	R/W
0x064	SRC_UPDATE	[7:0]	SRC_LOAD _SOURCE	RESERVED	SRC_ LOAD_ UPDATE	0x00	R/W

Register Details

Channel xx configuration register	Bits	Bit Name	Settings	Description	Reset	Access Type
Channel 0 configuration register Address:0x000; Reset：0x00; Name：CH0_CONFIG	[7:6]	CH0_GAIN		AFE Gain	0x0	R/W
			00	Gain1		
			01	Gain2		
			10	Gain4		
			11	Gain8		
	5	CH0_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH0_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	RESERVED		Reserved	0x0	R/W
Channel 1 configuration register Address:0x001; Reset：0x00; Name：CH1_CONFIG	[7:6]	CH1_GAIN		AFE Gain	0x0	R/W
			00	Gain1		
			01	Gain2		
			10	Gain4		
			11	Gain8		
	5	CH1_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH1_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	Reserved		Reserved	0x0	R/W

Channel xx configuration register	Bits	Bit Name	Settings	Description	Reset	Access Type
Channel 2 configuration register Address:0x002; Reset：0x00; Name：CH2_CONFIG	[7:6]	CH2_GAIN		AFE Gain	0x0	R/W
			00	Gain 1		
			01	Gain 2		
			10	Gain 4		
			11	Gain 8		
	5	CH2_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH2_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	Reserved		Reserved	0x0	R/W
Channel 3 configuration register Address:0x003; Reset：0x00; Name：CH3_CONFIG	[7:6]	CH3_GAIN		AFE Gain	0x0	R/W
			00	Gain 1		
			01	Gain 2		
			10	Gain 4		
			11	Gain 8		
	5	CH3_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH3_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	Reserved		Reserved	0x0	R/W
Channel 4 configuration register Address:0x004; Reset：0x00; Name：CH4_CONFIG	[7:6]	CH4_GAIN		AFE Gain	0x0	R/W
			00	Gain 1		
			01	Gain 2		
			10	Gain 4		
			11	Gain 8		
	5	CH4_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH4_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	Reserved		Reserved	0x0	R/W
Channel 5 configuration register Address:0x005;	[7:6]	CH5_GAIN		AFE Gain	0x0	R/W
			00	Gain 1		
			01	Gain 2		

Reset：0x00； Name：CH5_CONFIG			10	Gain 4		
			11	Gain 8		
	5	CH5_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH5_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	Reserved		Reserved	0x0	R/W
Channel 6 configuration register Address:0x004； Reset：0x00； Name：CH4_CONFIG	[7:6]	CH6_GAIN		AFE Gain	0x0	R/W
			00	Gain 1		
			01	Gain 2		
			10	Gain 4		
			11	Gain 8		
	5	CH6_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH6_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	Reserved		Reserved	0x0	R/W

Channel 7 configuration register Address:0x007； Reset：0x00； Name：CH7_CONFIG	[7:6]	CH7_GAIN		AFE Gain	0x0	R/W
			00	Gain 1		
			01	Gain 2		
			10	Gain 4		
			11	Gain 8		
	5	CH7_REF_MONITOR		Channel Used as Reference Monitor	0x0	R/W
	4	CH7_RX		Channel Meter Mux Rx Mode	0x0	R/W
	[3:0]	Reserved		Reserved	0x0	R/W

DISABLE CLOCKS TO ADC CHANNEL REGISTER Address: 0x008; Reset: 0x00; Name: CH_DISABLE	**Bits**	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
	7	CH7_DISABLE		Channel 7 Disable	0x0	R/W
	6	CH6_DISABLE		Channel 6 Disable	0x0	R/W
	5	CH5_DISABLE		Channel 5 Disable	0x0	R/W
	4	CH4_DISABLE		Channel 4 Disable	0x0	R/W
	3	CH3_DISABLE		Channel 3 Disable	0x0	R/W

	2	CH2_DISABLE		Channel 2 Disable	0x0	R/W
	1	CH1_DISABLE		Channel 1 Disable	0x0	R/W
	0	CH0_DISABLE		Channel 0 Disable	0x0	R/W
CHANNEL 0 SYNC OFFSET REGISTER Address: 0x009; Reset:0x00; Name:CH0_SYNC_OFFSET	[7:0]	CH0_SYNC_OFFSET		CH0_SYNC_OFFSET	0x0	R/W
CHANNEL 1 SYNC OFFSET REGISTER Address: 0x00A; Reset:0x00; Name:CH1_SYNC_OFFSET	[7:0]	CH1_SYNC_OFFSET		CH1_SYNC_OFFSET	0x0	R/W
CHANNEL 2 SYNC OFFSET REGISTER Address: 0x00B; Reset:0x00; Name:CH2_SYNC_OFFSET	[7:0]	CH2_SYNC_OFFSET		CH2_SYNC_OFFSET	0x0	R/W
CHANNEL 3 SYNC OFFSET REGISTER Address: 0x00C; Reset:0x00; Name:CH3_SYNC_OFFSET	[7:0]	CH3_SYNC_OFFSET		CH3_SYNC_OFFSET	0x0	R/W
CHANNEL 4 SYNC OFFSET REGISTER Address: 0x00D; Reset:0x00; Name:CH4_SYNC_OFFSET	[7:0]	CH4_SYNC_OFFSET		CH4_SYNC_OFFSET	0x0	R/W
CHANNEL 5 SYNC OFFSET REGISTER Address: 0x00E; Reset:0x00;	[7:0]	CH5_SYNC_OFFSET		CH5_SYNC_OFFSET	0x0	R/W

Name:CH5_SYNC_OFFSET						
CHANNEL 6 SYNC OFFSET REGISTER Address: 0x00F; Reset:0x00; Name:CH6_SYNC_OFFSET	[7:0]	CH6_SYNC_OFFSET		CH6_SYNC_OFFSET	0x0	R/W
CHANNEL 7 SYNC OFFSET REGISTER Address: 0x010; Reset:0x00; Name:CH7_SYNC_OFFSET	[7:0]	CH7_SYNC_OFFSET		CH7_SYNC_OFFSET	0x0	R/W

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
GENERAL USER CONFIGURATION 1 REGISTER Address: 0x011; Reset: 0x24; Name: GENERAL_USER_ CONFIG_1	7	ALL_CH_DIS_MCLK EN		If all Σ-Δ channels are disabled, setting this bit high allows DCLK to continue toggling.	0x0	R/W
	6	POWERMODE		Power Mode.	0x0	R/W
			0	Low power (1/4).		
			1	High resolution.		
	5	PDB_VCM		Power Down VCM Buffer. Active low.	0x1	R/W
	4	PDB_REFOUT_BUF		Power Down Internal Reference Output Buffer. Active low.	0x0	R/W
	3	PDB_SAR		Power Down SAR. Active low.	0x0	R/W
	2	PDB_RC_OSC		Power Down Signal for Internal Oscillator. Active low.	0x1	R/W
	[1:0]	SOFT_RESET	00 01 10 11	Soft Reset No effect No effect 2nd write 1st write	0x0	R/W
GENERAL USER	[7:6]	Reserved.		Reserved.	0x0	R/W

CONFIGURATION 2 REGISTER Address: 0x012；Reset: 0x09；Name: GENERAL_USER_CONFIG_2	5	SAR_DIAG_MODE_EN		Sets SPI Interface to Read Back SAR Result on SDO.	0x0	R/W
	[4:3]	SDO_DRIVE_STR		SDO Drive Strength.	0xl	R/W
			00	Nominal.		
			01	Strong.		
			10	Weak.		
			11	Extra strong.		
	[2:1]	DOUT_DRIVE_STR		DOUTx Drive Strength.	0x0	R/W
			00	Nominal.		
			01	Strong.		
			10	Weak.		
			11	Extra strong.		
	0	SPI_SYNC		SYNC Pulse Generated Through SPI.	0xl	R/W
			0	This signal is AND'ed with the value on the $\overline{\text{START}}$ pin in the control module and generates a pulse in the $\overline{\text{SYNC}}$_IN pin.		
			1	This bit is AND'ed with the value on $\overline{\text{START}}$ pin in the control module.		
GENERAL USER CONFIGURATION 3 REGISTER Address: 0x013；Reset: 0x80；Name: GENERAL_USER_CONFIG_3	[7:6]	CONVST_DEGLITCH_DIS		Disable deglitching of CONVST_SAR pin	0x2	R/W
			00	Reserved.		
			01	Reserved.		
			10	CONVST_SAR Deglitch 1.5 MCLK.		
			11	No deglitch circuit.		
	5	RESERVED		Reserved.	0x0	R/W
	4	SPI_SLAVE_MODE_EN		Enable to SPI slave mode to read back ADC on SDO	0x0	R/W
	[3:2]	RESERVED		Reserved.	0x0	R/W
	1	RESERVED		Reserved.	0x0	R/W
	0	CLK_QUAL_DIS		Disables the clock qualifier check if the	0x0	R/W

				user requires to use an MCLK signal <265 kHz.		
DATA OUTPUT FORMAT REGISTER Address: 0x014; Reset: 0x20; Name: DOUT_FORMAT	[7:6]	DOUT_FORMAT		Data Out Format.	0x0	R/W
			00	4 DOUT lines		
			01	2 DOUT lines		
			10	1 DOUT lines		
			11	1 DOUT lines		
	5	DOUT_HEADER_FORMAT		DOUT Header Format	0x1	R/W
			0	Status header		
			1	CRC header		
	4	RESERVED		Reserved.	0x0	R/W
	[3:1]	DCLK_CLK_DIV		Divide MCLK	0x0	R/W
			000	Divide by 1		
			001	Divide by 2		
			010	Divide by 4		
			011	Divide by 8		
			100	Divide by 16		
			101	Divide by 32		
			110	Divide by 64		
			111	Divide by 128		
	0			Reserved.	0x0	R/W
MAIN ADC METER AND REFERENCE MUX CONTROL REGISTER Address：0x015; Reset:0x00; Name：ADC_MUX_CONFIG	[7:6]	REF_MUX_CTRL		SD ADC Reference Mux	0x0	R/W
			00	External reference REFx+/REFx−		
			01	Internal reference.		
			10	External supply AVDD1x/AVSSx.		
			11	External reference REFx−/REFx+.		
	[5:2)	MTR_MUX_CTRL		SD ADC Meter Mux	0x0	R/W
			0010	280 mV		
			0011	External reference REFx+/REFx−		

			0100	External reference REFx−/REFx+		
			0101	External reference REFx−/REFx−		
			0110	Internal reference +/−		
			0111	Internal reference −/+		
			1000	Internal reference +/+		
			1001	External reference REFx+/REFx+		
	[1:0]	RESERVED		Reserved.	0x0	R/W

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
GLOBAL DIAGNOSTICS MUX REGISTER Address: 0x016; Reset: 0x00; Name:GLOBAL_MUX_CONFIG	[7:3]	GLOBAL_MUX_CTRL		Global SAR Diagnostics Mux Control.	0x0	R/W
			00000	AUXAIN+/AUXAIN-。		
			00001	DVBE/AVSSx。		
			00010	REF1+/REF1-。		
			10011	REF2+/REF2-。		
			10100	REF_OUTIAVSSx。		
			10101	VCM/AVSSx。		
			10110	AREG1CAP/AVSSx。		
			10111	AREG2CAP/AVSSx。		
			11000	DREGCAP/DGND。		
			11001	AVDD1A/AVSSx。		
			11010	AVDD1B/AVSSx。		
			11011	AVDD2A/AVSSx。		
			11100	AVDD2B/AVSSx。		
			11101	IOVDD/DGND。		
			11110	AVDD4/AVSSx。		
			11111	DGND/AVSS1A。		
			10000	DGND/AVSS1B。		
			10001	DGND/AVSSx。		
			10010	AVDD4/AVSSx。		

			10011	REF1+/AVSSx。		
			10100	REF2+/AVSSx。		
			10101	AVDD4/AVSSx. Attenuated.		
	[2:0]	RESERVED		Reserved.	0x0	R/W
GPIO CONFIGURATION REGISTER Address:0x017: Reset:0x00; Name:GPIO_CONFIG	[7:3]	RESERVED		Reserved.	0x0	R/W
	[2:0]	GPIO_OP_EN		GPIO Input/Output	0x0	R/W
GPIO DATA REGISTER Address:0x018; Reset:0x00; Name:GPIO_DATA	[7:6]	RESERVED		Reserved.	0x0	R/W
	[5:3]	GPIO_READ_DATA		Data Read from the GPIO Pins	0x0	R
	[2:0]	GPIO_WRITE_DATA		Value Sent to the GPIO Pins	0x0	R/W
BUFFER CONFIGURATION 1 REGISTER Address:0x019; Reset:0x38; Name: BUFFER CONFIG 1	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	REF_BUF_POS_EN		Reference Buffer Positive Enable	0xl	R/W
	3	REF_BUF_NEG_EN		Reference Buffer Negative Enable	0xl	R/W
	[2:0]	RESERVED		Reserved.	0x0	R/W
BUFFER CONFIGURATION 2 REGISTER Address:0x01A; Reset:0xC0; Name: BUFFER CONFIG 2	7	REFBUFP_PREQ		Reference Buffer Positive Precharge Enable	0xl	R/W
	6	REFBUFN PREQ		Reference Buffer Negative Precharge Enable	0xl	R/W
	[5:3]	RESERVED		Reserved.	0x0	R/W
	2	PDB_ALD01_OVRDRV		AREG1CAP Overdrive Enable	0x0	R/W
	1	PDB_ALD02_OVRDRV		AREG2CAP Overdrive Enable	0x0	R/W
	0	PDB_DLDO_OVRDRY		DREGCAP Overdrive Enable	0x0	R/W

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
CHANNEL 0 OFFSET UPPER BYTE REGISTER Address:0x01C; Reset:0x00; Name:CH0_OFFSET_UPPER_B	[7:0]	CH0_OFFSET_ALL[23:16]		Combined Offset Register Channel 0	0x0	R/W

YTE						
CHANNEL 0 OFFSET MIDDLE BYTE REGISTER Address:0x01D;Reset:0x00; Name:CH0_OFFSET_MID_BYTE	[7:0]	CH0_OFFSET_ALL[15:8]		Combined Offset Register Channel 0	0x0	R/W
CHANNEL 0 OFFSET LOWER BYTE REGISTER Address:0x01E;Reset:0x00; Name:CH0_OFFSET_LOWER_BYTE	[7:0]	CH0_OFFSET_ALL[7:0]		Combined Offset Register Channel 0	0x0	R/W
CHANNEL 0 GAIN UPPER BYTE REGISTER Address:0x01F:Reset:0x00; Name:CH0_GAIN_UPPER_BYTE	[7:0]	CH0_GAIN_ALL[23:16]		Combined Gain Register Channel 0	0x0	R/W
CHANNEL 0 GAIN MIDDLE BYTE REGISTER Address:0x020;Reset:0x00; Name:CH0 GAIN MID BYTE	[7:0]	CH0_GAIN_ALL[15:8]		Combined Gain Register Channel 0	0x0	R/W
CHANNEL 0 GAIN LOWER BYTE REGISTER Address:0x021;Reset:0x00; Name:CH0_GAIN_LOWER_BYTE	[7:0]	CH0_GAIN_ALL[7:0]		Combined Gain Register Channel 0	0x0	R/W
CHANNEL 1 OFFSET UPPER BYTE REGISTER Address:0x022;Reset:0x00; Name:CH1_OFFSET_UPPER_BYTE	[7:0]	CH1_OFFSET_ALL[23:16]		Combined Offset Register Channel 1	0x0	R/W
CHANNEL 1 OFFSET MIDDLE BYTE REGISTER Address:0x023;Reset:0x00;	[7:0]	CH1_OFFSET_ALL[15:8]		Combined Offset Register Channel 1	0x0	R/W

Name:CH1_OFFSET_MID_BY TE						
CHANNEL 1 OFFSET LOWER BYTE REGISTER Address:0x024;Reset:0x00; Name:CH1_OFFSET_LOWER_ BYTE	[7:0]	CH1_OFFSET_ALL[7:0]		Combined Offset Register Channel 1	0x0	R/W
CHANNEL 1 GAIN UPPER BYTE REGISTER Address:0x025;Reset:0x00; Name:CH1_GAIN_UPPER_BY TE	[7:0]	CH1_GAIN_ALL[23:16]		Combined Gain Register Channel 1	0x0	R/W
CHANNEL 1 GAIN MIDDLE BYTE REGISTER Address:0x026;Reset:0x00; Name:CH1_GAIN_MID_BYTE	[7:0]	CH1_GAIN_ALL[15:8]		Combined Gain Register Channel 1	0x0	R/W
CHANNEL 1 GAIN LOWER BYTE REGISTER Address:0x027;Reset:0x00; Name:CH1_GAIN_LOWER_BY TE	[7:0]	CH1_GAIN_ALL[7:0]		Combined Gain Register Channel 1	0x0	R/W
CHANNEL 2 OFFSET UPPER BYTE REGISTER Address:0x028;Reset:0x00; Name: CH2_OFFSET_UPPER_BYTE	[7:0]	CH2_OFFSET_ALL[23:16]		Combined Offset Register Channel 2	0x0	R/W
CHANNEL 2 OFFSET MIDDLE BYTE REGISTER Address:0x029;Reset:0x00; Name:CH2_OFFSET_MID_BY TE	[7:0]	CH2_OFFSET_ALL[15:8]		Combined Offset Register Channel 2	0x0	R/W
CHANNEL 2 OFFSET LOWER BYTE REGISTER	[7:0]	CH2_OFFSET_ALL[7:0]		Combined Offset Register Channel 2	0x0	R/W

Address:0x02A;Reset:0x00; Name:CH2 OFFSET LOWER BYTE						
CHANNEL 2 GAIN UPPER BYTE REGISTER Address:0x02B;Reset:0x00; Name:CH2_GAIN_UPPER_BY TE	[7:0]	CH2_GAIN_ALL[23:16]		Combined Gain Register Channel 2	0x0	R/W
CHANNEL 2 GAIN MIDDLE BYTE REGISTER Address:0x02C;Reset:0x00; Name:CH2_GAIN_MID_BYTE	[7:0]	CH2_GAIN_ALL[15:8]		Combined Gain Register Channel 2	0x0	R/W
CHANNEL 2 GAIN LOWER BYTE REGISTER Address:0x02D;Reset:0x00; Name:CH2_GAIN_LOWER_BY TE	[7:0]	CH2_GAIN_ALL[7:0]		Combined Gain Register Channel 2	0x0	R/W
CHANNEL 3 OFFSET UPPER BYTE REGISTER Address:0x02E;Reset:0x00; Name:CH3_OFFSET_UPPER_B YTE	[7:0]	CH3_OFFSET_ALL[23:16]		Combined Offset Register Channel 3	0x0	R/W
CHANNEL 3 OFFSET MIDDLE BYTE REGISTER Address:0x02F;Reset:0x00; Name:CH3_OFFSET_MID_BY TE	[7:0]	CH3_OFFSET_ALL[15:8]		Combined Offset Register Channel 3	0x0	R/W

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
CHANNEL 3 OFFSET LOWER BYTE REGISTER Address:0x030;Reset:0x00; Name:CH3_OFFSET_LOWER_	[7:0]	CH3_OFFSET_ALL[7:0]		Combined Offset Register Channel 3	0x0	R/W

BYTE						
CHANNEL 3 GAIN UPPER BYTE REGISTER Address:0x031;Reset:0x00; Name:CH3_GAIN_UPPER_BYTE	[7:0]	CH3_GAIN_ALL[23:16]		Combined Gain Register Channel 3	0x0	R/W
CHANNEL 3 GAIN MIDDLE BYTE REGISTER Address:0x032;Reset:0x00; Name:CH3_GAIN_MID_BYTE	[7:0]	CH3_GAIN_ALL[15:8]		Combined Gain Register Channel 3	0x0	R/W
CHANNEL 3 GAIN LOWER BYTE REGISTER Address:0x033;Reset:0x00; Name:CH3_GAIN_LOWER_BYTE	[7:0]	CH3_GAIN_ALL[7:0]		Combined Gain Register Channel 3	0x0	R/W
CHANNEL 4 OFFSET UPPER BYTE REGISTER Address:0x034;Reset:0x00; Name:CH4_OFFSET_UPPER_BYTE	[7:0]	CH4_OFFSET_ALL[23:16]		Combined Offset Register Channel 4	0x0	R/W
CHANNEL 4 OFFSET MIDDLE BYTE REGISTER Address:0x035;Reset:0x00; Name:CH4_OFFSET_MID_BYTE	[7:0]	CH4_OFFSET_ALL[15:8]		Combined Offset Register Channel 4	0x0	R/W
CHANNEL 4 OFFSET LOWER BYTE REGISTER Address:0x036;Reset:0x00; Name:CH4_OFFSET_LOWER_BYTE	[7:0]	CH4_OFFSET_ALL[7:0]		Combined Offset Register Channel 4	0x0	R/W
CHANNEL 4 GAIN UPPER BYTE REGISTER Address:0x037;Reset:0x00;	[7:0]	CH4_GAIN_ALL[23:16]		Combined Gain Register Channel 4	0x0	R/W

Name:CH4_GAIN_UPPER_BY TE						
CHANNEL 4 GAIN MIDDLE BYTE REGISTER Address:0x038;Reset:0x00; Name:CH4_GAIN_MID_BYTE	[7:0]	CH4_GAIN_ALL[15:8]		Combined Gain Register Channel 4	0x0	R/W
CHANNEL 4 GAIN LOWER BYTE REGISTER Address:0x039;Reset:0x00; Name:CH4_GAIN_LOWER_BY TE	[7:0]	CH4_GAIN_ALL[7:0]		Combined Gain Register Channel 4	0x0	R/W
CHANNEL 5 OFFSET UPPER BYTE REGISTER Address:0x03A;Reset:0x00; Name:CH5_OFFSET_UPPER_B YTE	[7:0]	CH5_OFFSET_ALL[23:16]		Combined Offset Register Channel 5	0x0	R/W
CHANNEL 5 OFFSET MIDDLE BYTE REGISTER Address:0x03B;Reset:0x00; Name:CH5_OFFSET_MID_BY TE	[7:0]	CH5_OFFSET_ALL[15:8]		Combined Offset Register Channel 5	0x0	R/W
CHANNEL 5 OFFSET LOWER BYTE REGISTER Address:0x03C;Reset:0x00; Name:CH5_OFFSET_LOWER_ BYTE	[7:0]	CH5_OFFSET_ALL[7:0]		Combined Offset Register Channel 5	0x0	R/W
CHANNEL 5 GAIN UPPER BYTE REGISTER Address:0x03D;Reset:0x00; Name:CH5_GAIN_UPPER_BY TE	[7:0]	CH5_GAIN_ALL[23:16]		Combined Gain Register Channel 5	0x0	R/W
CHANNEL 5 GAIN MIDDLE BYTE REGISTER	[7:0]	CH5_GAIN_ALL[15:8]		Combined Gain Register Channel 5	0x0	R/W

Address:0x03E;Reset:0x00; Name:CH5_GAIN_MID_BYTE						
CHANNEL 5 GAIN LOWER BYTE REGISTER Address:0x03F;Reset:0x00; Name:CH5_GAIN_LOWER_BYTE	[7:0]	CH5_GAIN_ALL[7:0]		Combined Gain Register Channel 5	0x0	R/W
CHANNEL 6 OFFSET UPPER BYTE REGISTER Address:0x040;Reset:0x00; Name:CH6_OFFSET_UPPER_BYTE	[7:0]	CH6_0FFSET_ALL[23:16]		Combined Offset Register Channel 6	0x0	R/W
CHANNEL 6 OFFSET MIDDLE BYTE REGISTER Address:0x041;Reset:0x00; Name:CH6_OFFSET_MID_BYTE	[7:0]	CH6_OFFSET_ALL[15:8]		Combined Offset Register Channel 6	0x0	R/W
CHANNEL 6 OFFSET LOWER BYTE REGISTER Address:0x042;Reset:0x00; Name:CH6_OFFSET_LOWER_BYTE	[7:0]	CH6_OFFSET_ALL[7:0]		Combined Offset Register Channel 6	0x0	R/W
CHANNEL 6 GAIN UPPER BYTE REGISTER Address:0x043;Reset:0x00; Name:CH6_GAIN_UPPER_BYTE	[7:0]	CH6_GAIN_ALL[23:16]		Combined Gain Register Channel 6	0x0	R/W

	Bits	Bit Name	Settings	Description	Reset	Access Type
CHANNEL 6 GAIN MIDDLE BYTE REGISTER Address:0x044;Reset:0x00; Name:CH6_GAIN_MID_BYTE	[7:0]	CH6_GAIN_ALL[15:8]		Combined Gain Register Channel 6	0x0	R/W

CHANNEL 6 GAIN LOWER BYTE REGISTER Address:0x045;Reset:0x00; Name:CH6_GAIN_LOWER_BYTE	[7:0]	CH6_GAIN_ALL[7:0]		Combined Gain Register Channel 6	0x0	R/W
CHANNEL 7 OFFSET UPPER BYTE REGISTER Address:0x046;Reset:0x00; Name:CH7_OFFSET_UPPER_BYTE	[7:0]	CH7_OFFSET_ALL[23:16]		Combined Offset Register Channel 7	0x0	R/W
CHANNEL 7 OFFSET MIDDLE BYTE REGISTER Address:0x047;Reset:0x00; Name:CH7_OFFSET_MID_BYTE	[7:0]	CH7_OFFSET_ALL[15:8]		Combined Offset Register Channel 7	0x0	R/W
CHANNEL 7 OFFSET LOWER BYTE REGISTER Address:0x048;Reset:0x00; Name:CH7_OFFSET_LOWER_BYTE	[7:0]	CH7_OFFSET_ALL[7:0]		Combined Offset Register Channel 7	0x0	R/W
CHANNEL 7 GAIN UPPER BYTE REGISTER Address:0x049;Reset:0x00; Name:CH7_GAIN_UPPER_BYTE	[7:0]	CH7_GAIN_ALL[23:16]		Combined Gain Register Channel 7	0x0	R/W
CHANNEL 7 GAIN MIDDLE BYTE REGISTER Address:0x04A;Reset:0x00; Name:CH7_GAIN_MID_BYTE	[7:0]	CH7_GAIN_ALL[15:8]		Combined Gain Register Channel 7	0x0	R/W
CHANNEL 7 GAIN LOWER BYTE REGISTER Address:0x04B;Reset:0x00; Name:CH7_GAIN_LOWER_BY	[7:0]	CH7_GAIN_ALL[7:0]		Combined Gain Register Channel 7	0x0	R/W

TE						

	Bits	Bit Name	Settings	Description	Reset	Access Type
CHANNEL 0 STATUS REGISTER Address:0x04C;Reset:0x00; Name:CH0_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH0_ERR_AINM_UV		Channel 0—AIN0− Undervoltage Error	0x0	R
	3	CH0_ERR_AINM_OV		Channel 0—AIN0− Overvoltage Error	0x0	R
	2	CH0_ERR_AINP_UV		Channel 0—AIN0+ Undervoltage Error	0x0	R
	1	CH0_ERR_AINP_OV		Channel 0—AIN0+ Overvoltage Error	0x0	R
	0	CH0_ERR_REF_DET		Channel 0—Reference Detect Error	0x0	R
CHANNEL 1 STATUS REGISTERAddress:0x04D; Reset:0x00; Name:CHI_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH1_ERR_AINM_UV		Channel 1—AIN1− Undervoltage Error	0x0	R
	3	CH1_ERR_AINM_OV		Channel 1—AIN1− Overvoltage Error	0x0	R
	2	CH1_ERR_AINP_UV		Channel 1—AIN1+ Undervoltage Error	0x0	R
	1	CH1_ERR_AINP_OV		Channel 1—AIN1+ Overvoltage Error	0x0	R
	0	CH1_ERR_REF_DET		Channel 1—Reference Detect Error	0x0	R
CHANNEL 2 STATUS REGISTER Address:0x04E;Reset:0x00; Name:CH2_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH2_ERR_AINM_UV		Channel 2—AIN2− Undervoltage Error	0x0	R
	3	CH2_ERR_AINM_OV		Channel 2—AIN2− Overvoltage Error	0x0	R
	2	CH2_ERR_AINP_UV		Channel 2—AIN2+ Undervoltage Error	0x0	R
	1	CH2_ERR_AINP_OV		Channel 2—AIN2+ Overvoltage Error	0x0	R
	0	CH2_ERR_REF_DET		Channel 2—Reference Detect Error	0x0	R

	Bits	Bit Name	Settings	Description	Reset	Access Type
CHANNEL 3 STATUS REGISTER Address:0x04F;Reset:0x00; Name:CH3_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH3_ERR_AINM_UV		Channel 3—AIN3− Undervoltage Error	0x0	R
	3	CH3_ERR_AINM_OV		Channel 3—AIN3− Overvoltage Error	0x0	R
	2	CH3_ERR_AINP_UV		Channel 3—AIN3+ Undervoltage Error	0x0	R
	1	CH3_ERR_AINP_OV		Channel 3—AIN3+ Overvoltage Error	0x0	R
	0	CH3_ERR_REF_DET		Channel 3—Reference Detect Error	0x0	R

CHANNEL 4 STATUS REGISTER Address:0x050;Reset:0x00; Name:CH4_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH4_ERR_AINM_UV		Channel 4—AIN4− Undervoltage Error	0x0	R
	3	CH4_ERR_AINM_OV		Channel 4—AIN4− Overvoltage Error	0x0	R
	2	CH4_ERR_AINP_UV		Channel 4—AIN4+ Undervoltage Error	0x0	R
	1	CH4_ERR_AINP_OV		Channel 4—AIN4+ Overvoltage Error	0x0	R
	0	CH4_ERR_REF_DET		Channel 4—Reference Detect Error	0x0	R
CHANNEL 5 STATUS REGISTER Address:0x051;Reset:0x00; Name:CH5_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH5_ERR_AINM_UV		Channel 5—AIN5− Undervoltage Error	0x0	R
	3	CH5_ERR_AINM_OV		Channel 5—AIN5− Overvoltage Error	0x0	R
	2	CH5_ERR_AINP_UV		Channel 5—AIN5+ Undervoltage Error	0x0	R
	1	CH5_ERR_AINP_OV		Channel 5—AIN5+ Overvoltage Error	0x0	R
	0	CH5_ERR_REF_DET		Channel 5—Reference Detect Error	0x0	R
CHANNEL 6 STATUS REGISTER Address:0x052;Reset:0x00; Name:CH6_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH6_ERR_AINM_UV		Channel 6—AIN6− Undervoltage Error	0x0	R
	3	CH6_ERR_AINM_OV		Channel 6—AIN6− Overvoltage Error	0x0	R
	2	CH6_ERR_AINP_UV		Channel 6—AIN6+ Undervoltage Error	0x0	R
	1	CH6_ERR_AINP_OV		Channel 6—AIN6+ Overvoltage Error	0x0	R
	0	CH6_ERR_REF_DET		Channel 6—Reference Detect Error	0x0	R
CHANNEL 7 STATUS REGISTER Address:0x053;Reset:0x00; Name:CH7_ERR_REG	[7:5]	RESERVED		Reserved.	0x0	R/W
	4	CH7_ERR_AINM_UV		Channel 7—AIN7− Undervoltage Error	0x0	R
	3	CH7_ERR_AINM_OV		Channel 7—AIN7− Overvoltage Error	0x0	R
	2	CH7_ERR_AINP_UV		Channel 7—AIN7+ Undervoltage Error	0x0	R
	1	CH7_ERR_AINP_OV		Channel 7—AIN7+ Overvoltage Error	0x0	R
	0	CH7_ERR_REF_DET		Channel 7—Reference Detect Error	0x0	R

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
CHANNEL 0/CHANNEL 1 DSP ERRORS REGISTER Address:0x054;Reset:0x00;	5	CH1_ERR_MOD_SAT		Channel 1—Modulator Output Saturation Error	0x0	R
	4	CH1_ERR_FILTER_SAT		Channel 1—Filter result has exceeded a	0x0	R

Name:CH0_1_SAT_ERR				reasonable level, before offset and gain calibration has been applied		
	3	CH1_ERR_OUTPUT_SAT		Channel 1—ADC conversion has exceeded limits and has been clamped	0x0	R
	2	CHO_ERR_MOD_SAT		Channel 0—Modulator Output Saturation Error	0x0	R
	1	CHO_ERR_FILTER_SAT		Channel 0—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
	0	CHO_ERR_OUTPUT_SAT		Channel 0—ADC conversion has exceeded limits and has been clamped	0x0	R
	Bits	Bit Name	Settings	Description	Reset	Access Type
CHANNEL 2/CHANNEL 3 DSP ERRORS REGISTER Address:0x055;Reset:0x00; Name:CH2_3_SAT_ERR	5	CH3_ERR_MOD_SAT		Channel 3—Modulator Output Saturation Error	0x0	R
	4	CH3_ERR_FILTER_SAT		Channel 3—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
	3	CH3_ERR_OUTPUT_SAT		Channel 3—ADC conversion has exceeded limits and has been clamped		
	2	CH2_ERR_MOD_SAT		Channel 2—Modulator Output Saturation Error	0x0	R
	1	CH2_ERR_FILTER_SAT		Channel 2—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
	0	CH2_ERR_OUTPUT_SAT		Channel 2—ADC conversion has exceeded limits and has been clamped		
CHANNEL 4/CHANNEL 5 DSP ERRORS REGISTER Address:0x056;Reset:0x00; Name:CH4_5_SAT_ERR	5	CH5_ERR_MOD_SAT		Channel 5—Modulator Output Saturation Error	0x0	R
	4	CH5_ERR_FILTER_SAT		Channel 5—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R

	3	CH5_ERR_OUTPUT_SAT		Channel 5—ADC conversion has exceeded limits and has been clamped	0x0	R
	2	CH4_ERR_MOD_SAT		Channel 4—Modulator Output Saturation Error	0x0	R
	1	CH4_ERR_FILTER_SAT		Channel 4—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
	0	CH4_ERR_OUTPUT_SAT		Channel 4—ADC conversion has exceeded limits and has been clamped	0x0	R
CHANNEL 6/CHANNEL 7 DSP ERRORS REGISTER Address:0x057;Reset:0x00; Name:CH6_7_SAT_ERR	5	CH7_ERR_MOD_SAT		Channel 7—Modulator Output Saturation Error	0x0	R
	4	CH7_ERR_FILTER_SAT		Channel 7—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
	3	CH7_ERR_OUTPUT_SAT		Channel 7—ADC conversion has exceeded limits and has been clamped	0x0	R
	2	CH6_ERR_MOD_SAT		Channel 6—Modulator Output Saturation Error	0x0	R
	1	CH6_ERR_FILTER_SAT		Channel 6—Filter result has exceeded a reasonable level, before offset and gain calibration has been applied	0x0	R
	0	CH6_ERR_OUTPUT_SAT		Channel 6—ADC conversion has exceeded limits and has been clamped	0x0	R
CHANNEL 0 TO CHANNEL 7 ERROR REGISTER ENABLE REGISTER Address:0x058;Reset:0xFE; Name:CHX_ERR_REG_EN	7	OUTPUT_SAT_TEST_EN		ADC Conversion Error Test Enable	0xl	R/W
	6	FILTER_SAT_TEST_EN		Filter Saturation Test Enable	0xl	R/W
	5	MOD_SAT_TEST_EN		Enable Error Flag for Modulator Saturation	0xl	R/W
	4	AINM_UV_TEST_EN		AINx− Undervoltage Test Enable	0xl	R/W
	3	AINM_OV_TEST_EN		AINx− Overvoltage Test Enable	0xl	R/W
	2	AINP_UV_TEST_EN		AINx+ Undervoltage Test Enable	0xl	R/W
	1	AINP_OV_TEST_EN		AINx+ Overvoltage Test Enable	0xl	R/W

	0	REF_DET_TEST_EN		Reference Detect Test Enable	0x0	R/W

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
GENERAL ERRORS REGISTER 1 Address:0x059;Reset:0x00; Name:GEN_ERR_REG 1	5	MEMMAP_CRC_ERR		A CRC of the memory map contents is run periodically to check for errors	0x0	R
	4	ROM_CRC_ERR		A CRC of the fuse contents is run periodically to check for errors in the fuses	0x0	R
	3	SPI_CLK_COUNT_ERR		SPI clock counter error	0x0	R
	2	SPI_INVALID_READ_ERR		SPI invalid read address	0x0	R
	1	SPI_INVALID_WRITE_ERR		SPI invalid write address	0x0	R
	0	SPI_CRC_ERR		SPI CRC error	0x0	R
	Bits	Bit Name	Settings	Description	Reset	Access Type
GENERAL ERRORS REGISTER 1 ENABLE Address:0x05A;Reset:0x3E; Name:GEN_ERR_REG_1_EN	5	MEMMAP_CRC_TEST_ERR		Memory Map CRC Test Enable	0xl	R/W
	4	ROM_CRC_TEST_ERR		Fuse CRC Test Enable	0xl	R/W
	3	SPI_CLK_COUNT_TEST_ERR		SPI Clock Counter Test Enable	0xl	R/W
	2	SPI_INVALID_READ_TEST_ERR		SPI Invalid Read Address Test Enable	0xl	R/W
	1	SPI_INVALID_WRITE_TEST_ERR		SPI Invalid Write Address Test Enable	0xl	R/W
	0	SPI_CRC_TEST_ERR		SPI CRC Error Test Enable	0x0	R/W
GENERAL ERRORS REGISTER 2 Address:0x05B;Reset:0x00; Name:GEN_ERR_REG_2	5	RESET DETECTED		Reset Detected	0x0	R
	4	EXT MCLK SWITCH ERR		Clock Not Switched Over	0x0	R
	2	ALD01 PSM ERR		AREG1CAP Power Supply Error	0x0	R
	1	ALDO2 PSM ERR		AREG2CAP Power Supply Error	0x0	R
	0	DLDO PSM ERR		DREGCAP Power Supply Error	0x0	R
GENERAL ERRORS	5	RESET_DETECT_EN		Reset Detect Enable	0xl	R/W

REGISTER 2 ENABLE Address:0x05C;Reset:0x3C; Name:GEN_ERR_REG_2_EN	4	RESERVED		Reserved	0xl	R/W
	[3:2]	LDO_PSM_TEST_EN		LDO PSM Test EN	0x3	R/W
			0	00—no power supply monitor test enabled.		
			1	01—run power supply monitor test on AREGxCAP		
			10	10—run power supply monitor test on DREGCAP		
			11	11—run power supply monitor test on all LDOs		
	[1:0]	LDO_PSM_TRIP_TEST_EN		LDO PSM Trip Test Enable	0x0	R/W
			0	00—no trip detect test enabled		
			1	01—run trip detect test on AREG1CAP		
			10	10—run trip detect test on AREG2CAP		
			11	11—run trip detect test on DREGCAP		

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
ERROR STATUS REGISTER 1 Address: 0x05D;Reset:0x00; Name:STATUS_REG_1	5	CHIP_ERROR		Set this bit high if any error bit is high	0x0	R
	4	ERR_LOC_CH4		An error specific to CH4_ERR_REG is active	0x0	R
	3	ERR_LOC_CH3		An error specific to CH3_ERR_REG is active	0x0	R
	2	ERR_LOC_CH2		An error specific to CH2_ERR_REG is active	0x0	R
	1	ERR_LOC_CH1		An error specific to CH1_ERR_REG is active	0x0	R
	0	ERR_LOC_CH0		An error specific to CH0_ERR_REG is active	0x0	R
ERROR STATUS REGISTER 2 Address: 0x05E;Reset:0x00;	5	CHIP_ERROR		Set high if any error bit is high	0x0	R
	4	ERR_LOC_GEN2		An error specific to GEN_ERR_REG_2 is	0x0	R

Name:STATUS_REG_2				active		
	3	ERR_LOC_GEN1		An error specific to GEN_ERR_REG_1 is active	0x0	R
	2	ERR_LOC_CH7		An error specific to CH7_ERR_REG is active	0x0	R
	1	ERR_LOC_CH6		An error specific to CH6_ERR_REG is active	0x0	R
	0	ERR_LOC_CH5		An error specific to CH5_ERR_REG is active	0x0	R

	Bits	**Bit Name**	**Settings**	**Description**	**Reset**	**Access Type**
ERROR STATUS REGISTER 3 Address: 0x05F;Reset:0x00; Name:STATUS_REG_3	5	CHIP_ERROR		Set high if any error bit is high.	0x0	R
	4	INIT_COMPLETE		Fuse initialization is complete. Device is ready to receive commands.	0x0	R
	3	ERR_LOC_SAT_CH6_7		An error specific to CH6_7_SAT_ERR register is active.	0x0	R
	2	ERR_LOC_SAT_CH4_5		An error specific to CH4_5_SAT_ERR register is active.	0x0	R
	1	ERR_LOC_SAT_CH2_3		An error specific to CH2_3_SAT_ERR register is active.	0x0	R
	0	ERR_LOC_SAT_CH0_1		An error specific to CH0_1_SAT_ERR register is active.	0x0	R

	Bits	Bit Name	Settings	Description	Reset	Access Type
DECIMATION RATE (N) LSB REGISTER Address:0x060;Reset:0x00;Name:SRC_N_MSB	[3:0]	SRC_N_ALL[11:8]		SRC N Combined	0x0	R/W
DECIMATION RATE (N) LSB	[7:0]	SRC_N_ALL[7:0]		SRC N Combined	0x0	R/W

REGISTER Address:0x061;Reset:0x80;Name :SRC_N_LSB						
DECIMATION RATE (IF) MSB REGISTER Address:0x062;Reset:0x00;Name :SRC_IF_MSB	[7:0]	SRC_IF_ALL[15:8]		SRC IF All	0x0	R/W
DECIMATION RATE (IF) LSB REGISTER Address:0x063;Reset:0x00;Name :SRC_IF_LSB	[7:0]	SRC_IF_ALL[7:0]		SRC IF All	0x0	R/W

	Bits	Bit Name	Settings	Description	Reset	Access Type
SRC LOAD SOURCE AND LOAD UPDATE REGISTER Address:0x064;Reset:0x00; Name:SRC_UPDATE	7	SRC_LOAD_SOURCE		Selects which option to load an SRC update	0x0	R/W
	0	SRC_LOAD_UPDATE		Asserts bit to load SRC registers into SRC	0x0	R/W

Typical Application Circuit Diagram

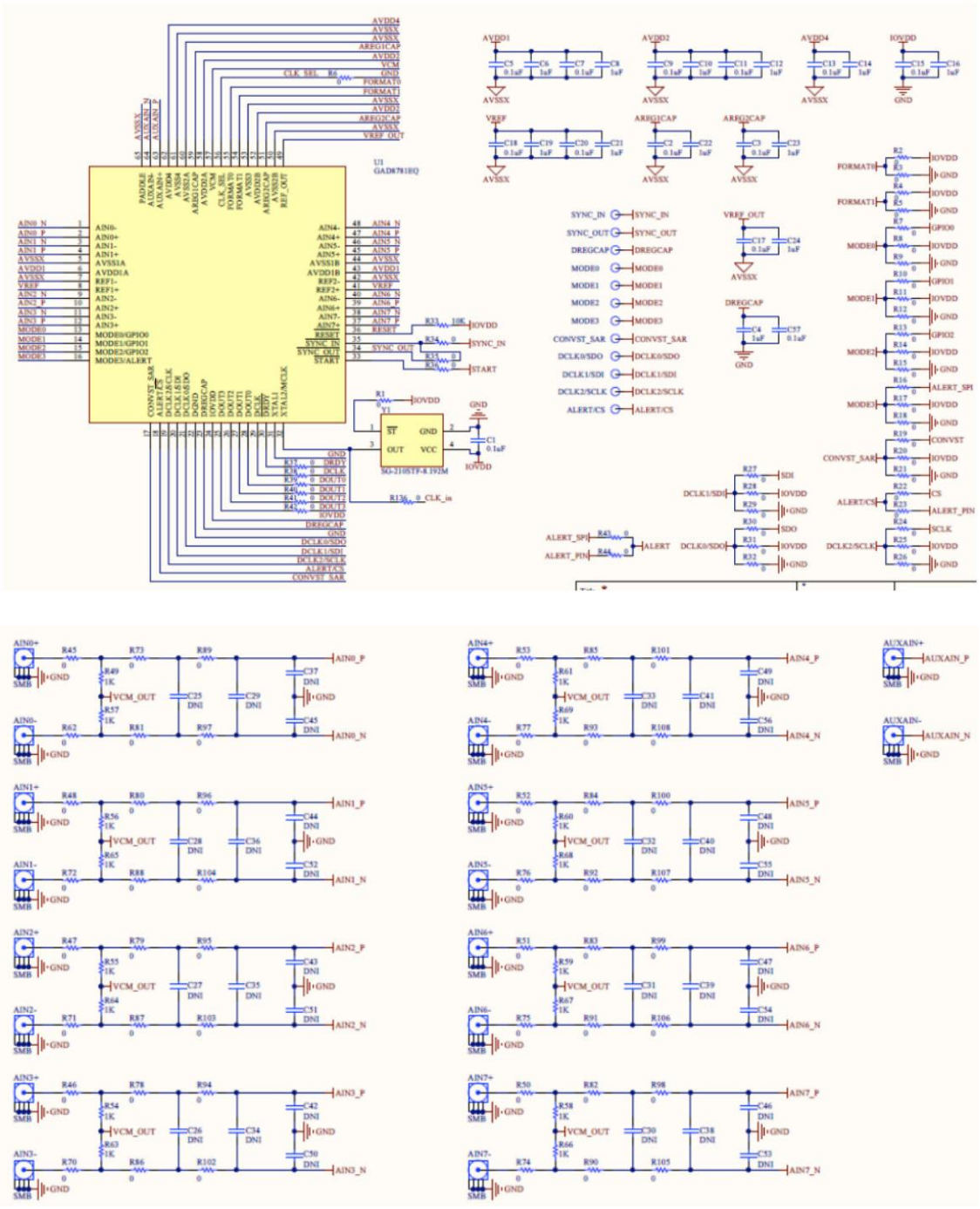

Figure 9. Typical Application Circuit Diagram

Note

1,Product installation precautions:

1) When using, do not insert the circuit backwards, otherwise it may cause circuit damage.

2) Require the application object circuit board to have a complete and clean ground.

3) The application object is required to be a multi-layer wiring board and contain independent layers.

4) It is required to separate the digital ground and analog ground of the application object circuit board as much as possible, and not place the digital line next to the analog line or under the ADC.

5) The power supply should be connected to high-quality ceramic bypass capacitors, and the bypass capacitors should be as close as possible to the pins. The shorter and wider the connection between the pins and the bypass capacitor, the better.

2,Precautions for product use:

1) Differential inputs should be as close and parallel as possible.

2) The input wiring should be as short as possible to minimize parasitic capacitance and noise introduction.

In order to achieve better heat dissipation and electrical performance, the bottom plate of the chip should be welded to a large ground end of the PCB board, in order to maximize the thermal performance of the package.

3) 3,Product protection precautions:

1) Electrostatic charges can easily accumulate on the human body and testing equipment, and may discharge unnoticed. Although this product has a dedicated ESD protection circuit, permanent device damage may occur when encountering high-energy electrostatic discharge. Therefore, it is recommended to take appropriate ESD prevention measures to avoid device performance degradation or loss of function.

2) Exceeding the absolute maximum rating may result in permanent damage to the device. This is only the maximum rated value and does not mean that the device can operate normally under these conditions or any other conditions beyond those shown in this product manual. Long term operation under absolute maximum rated conditions can affect the reliability of the device.

Common Faults and Solutions

1. No signal output: Check if the power voltage, input signal, and clock are correctly loaded

2. Overflow signal occurs: Check if the benchmark is working properly and if the input signal amplitude is correct.

3. Unstable device operation: Check the power supply to ensure stable power supply voltage.